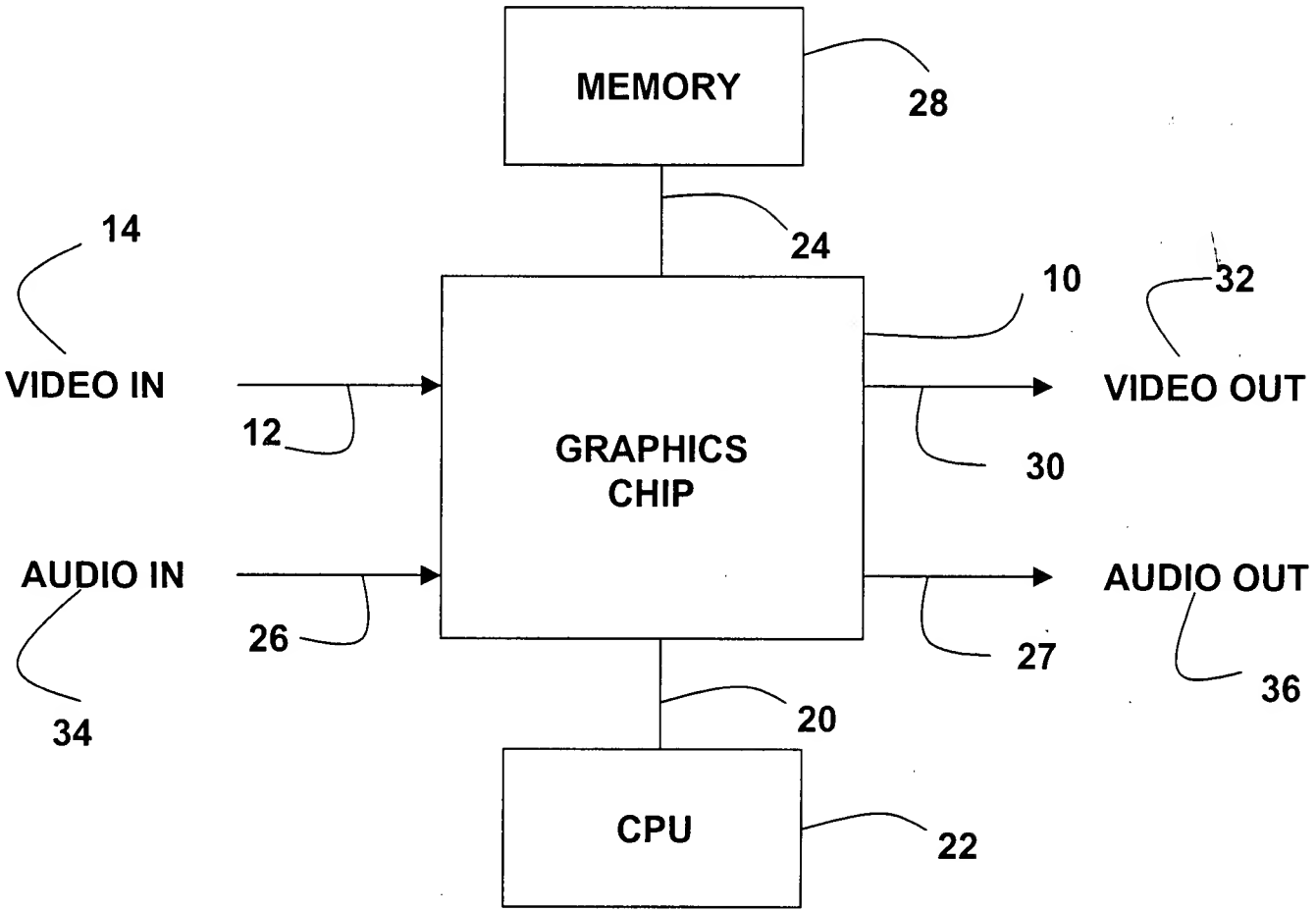

FIG. 1

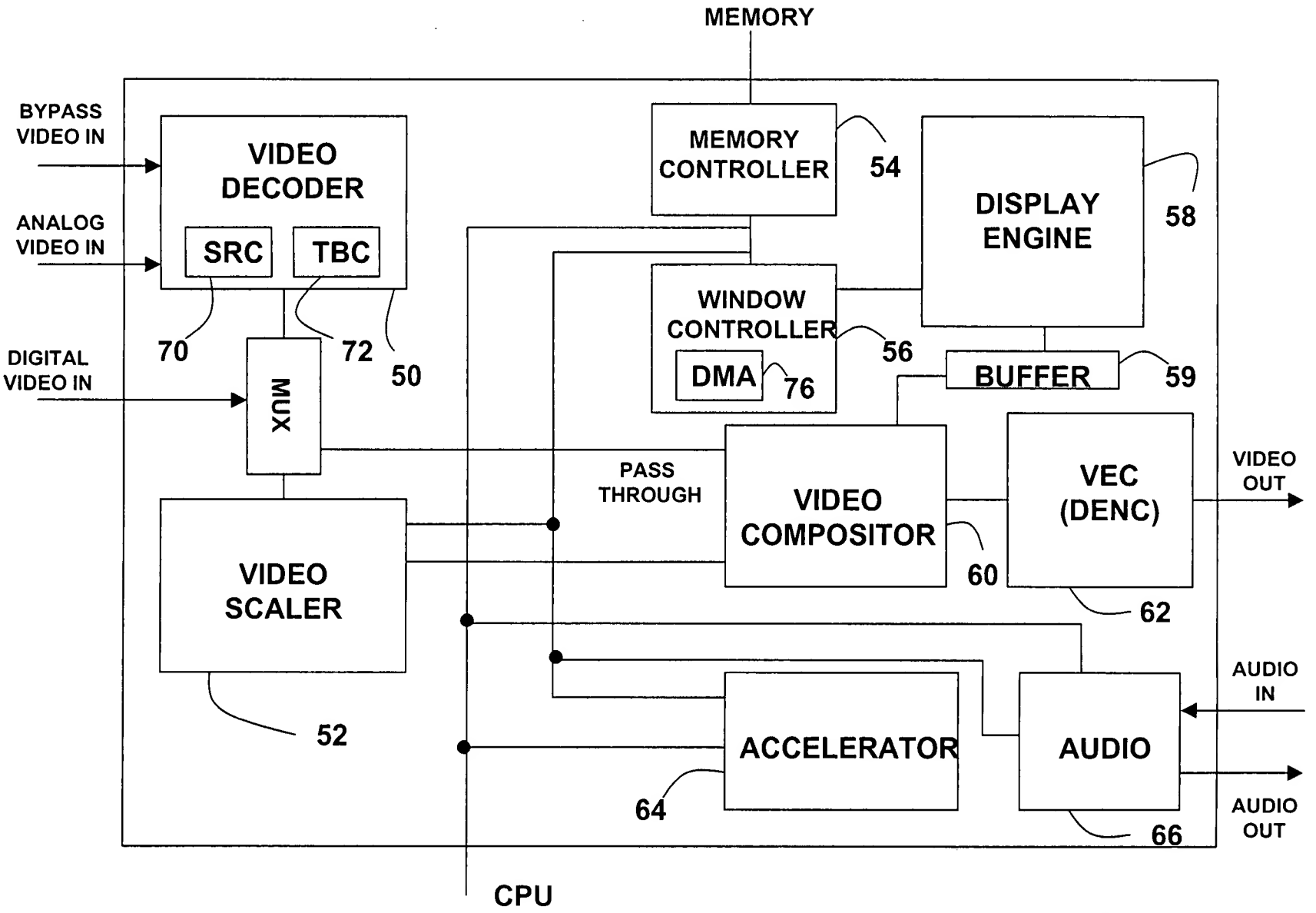

FIG. 2

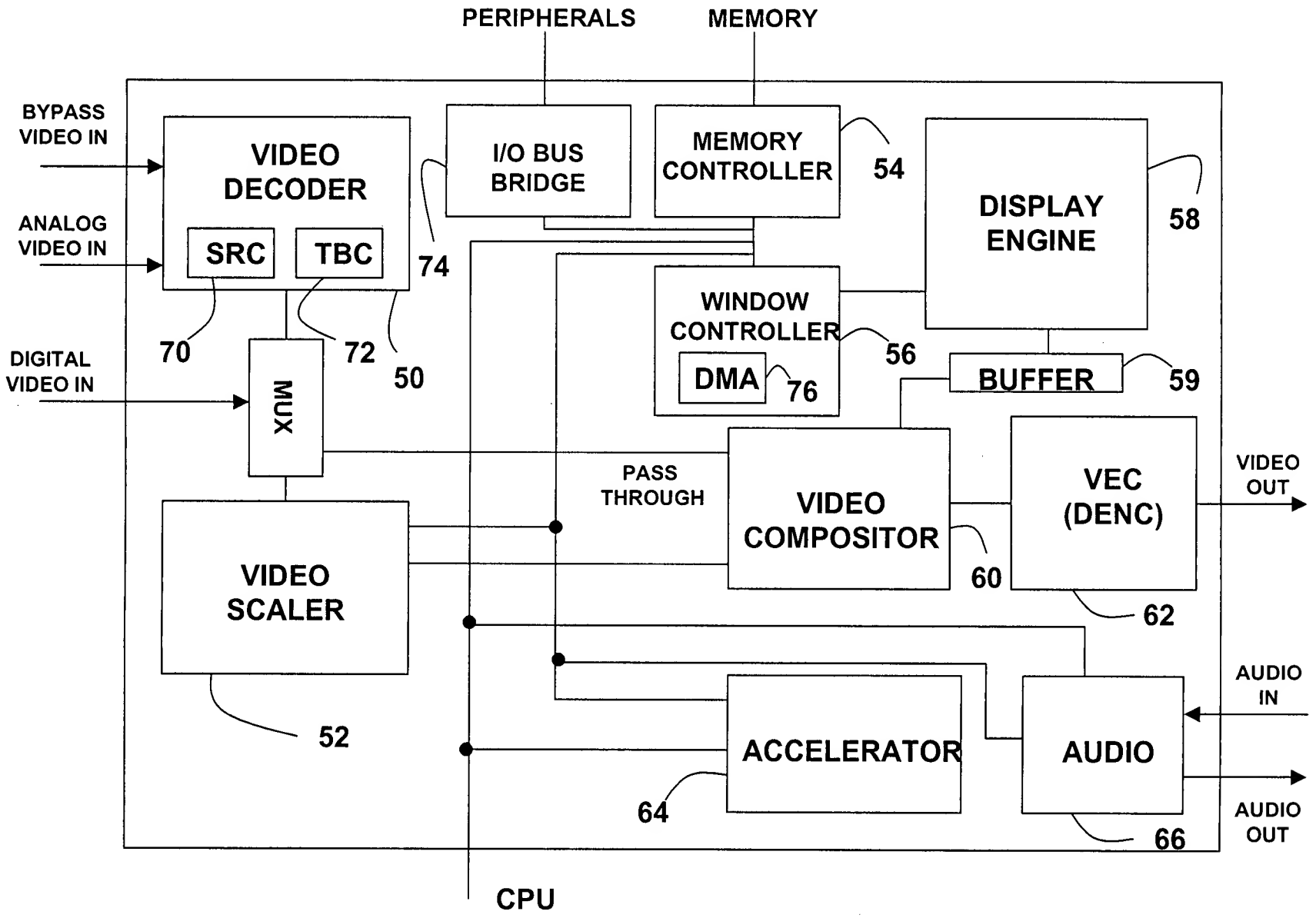

FIG. 3

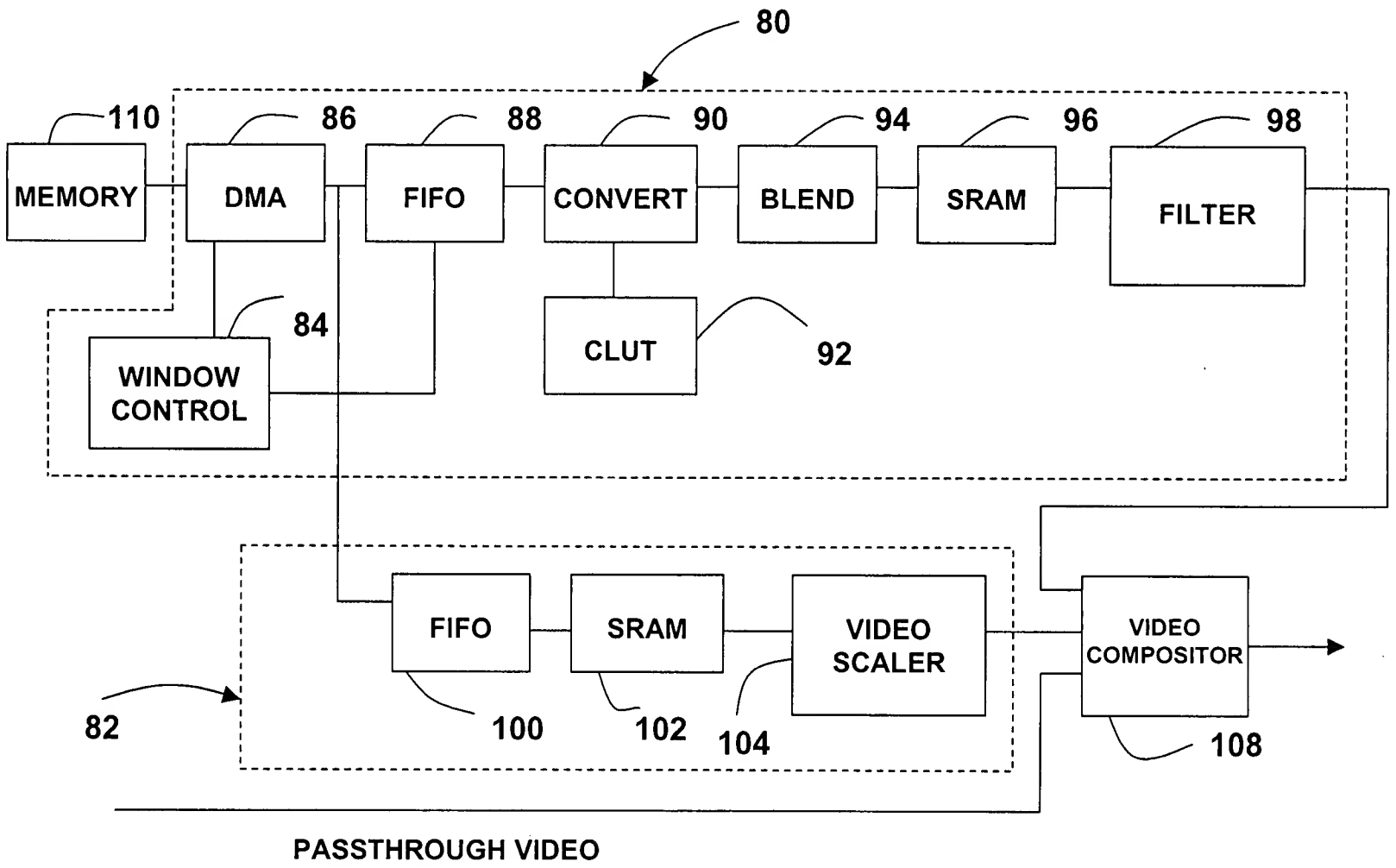

FIG. 4

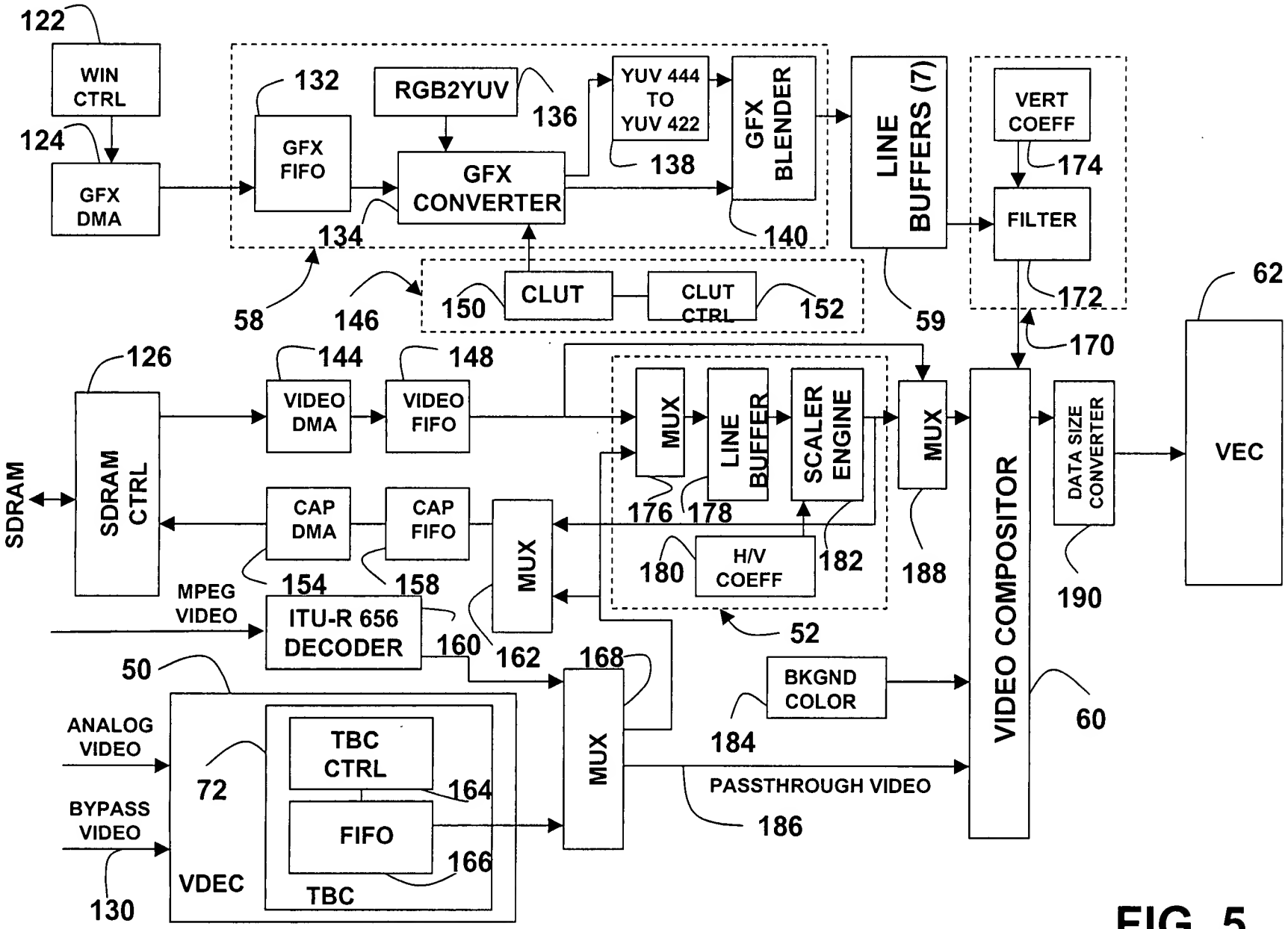

FIG. 5

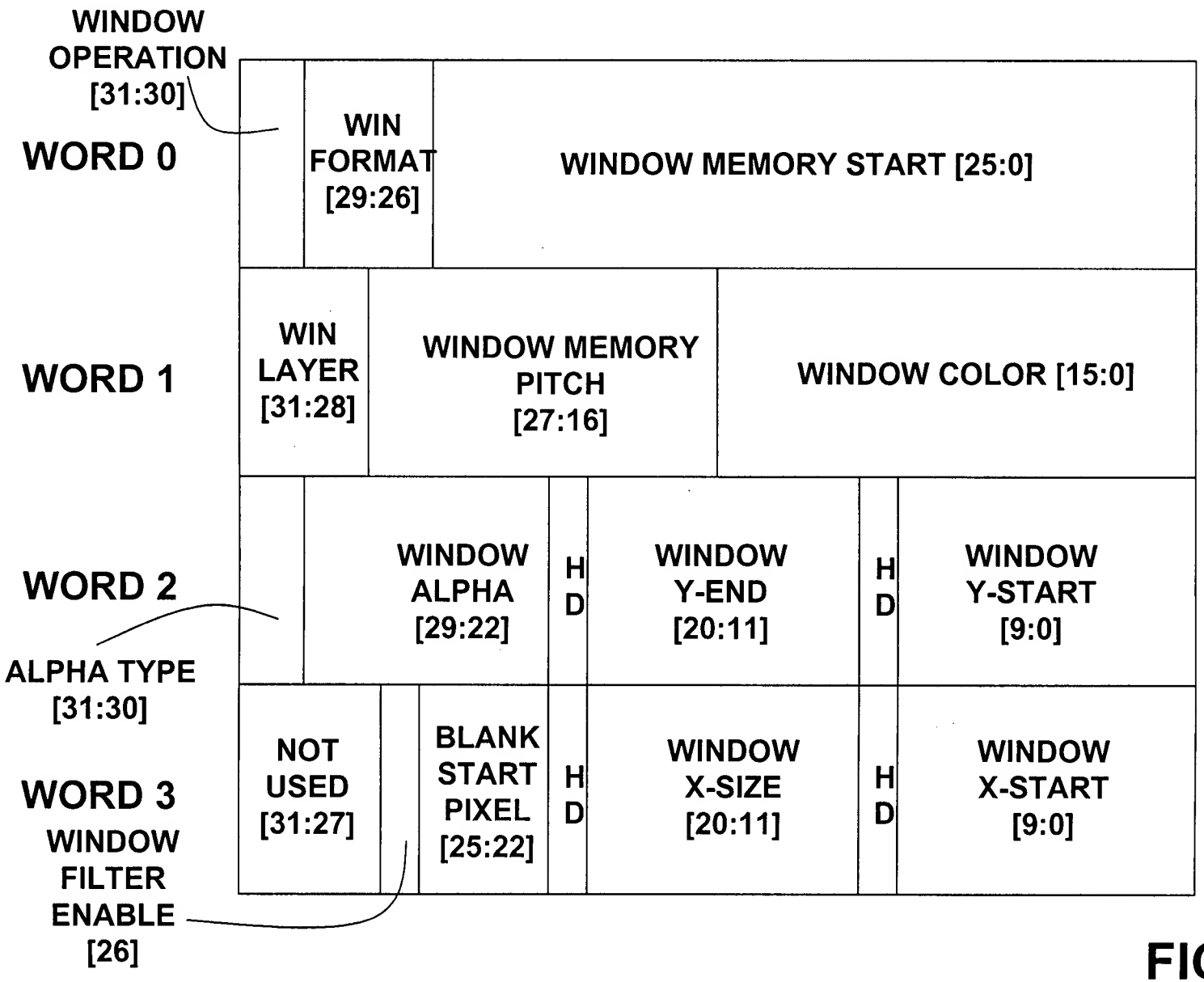

FIG. 6

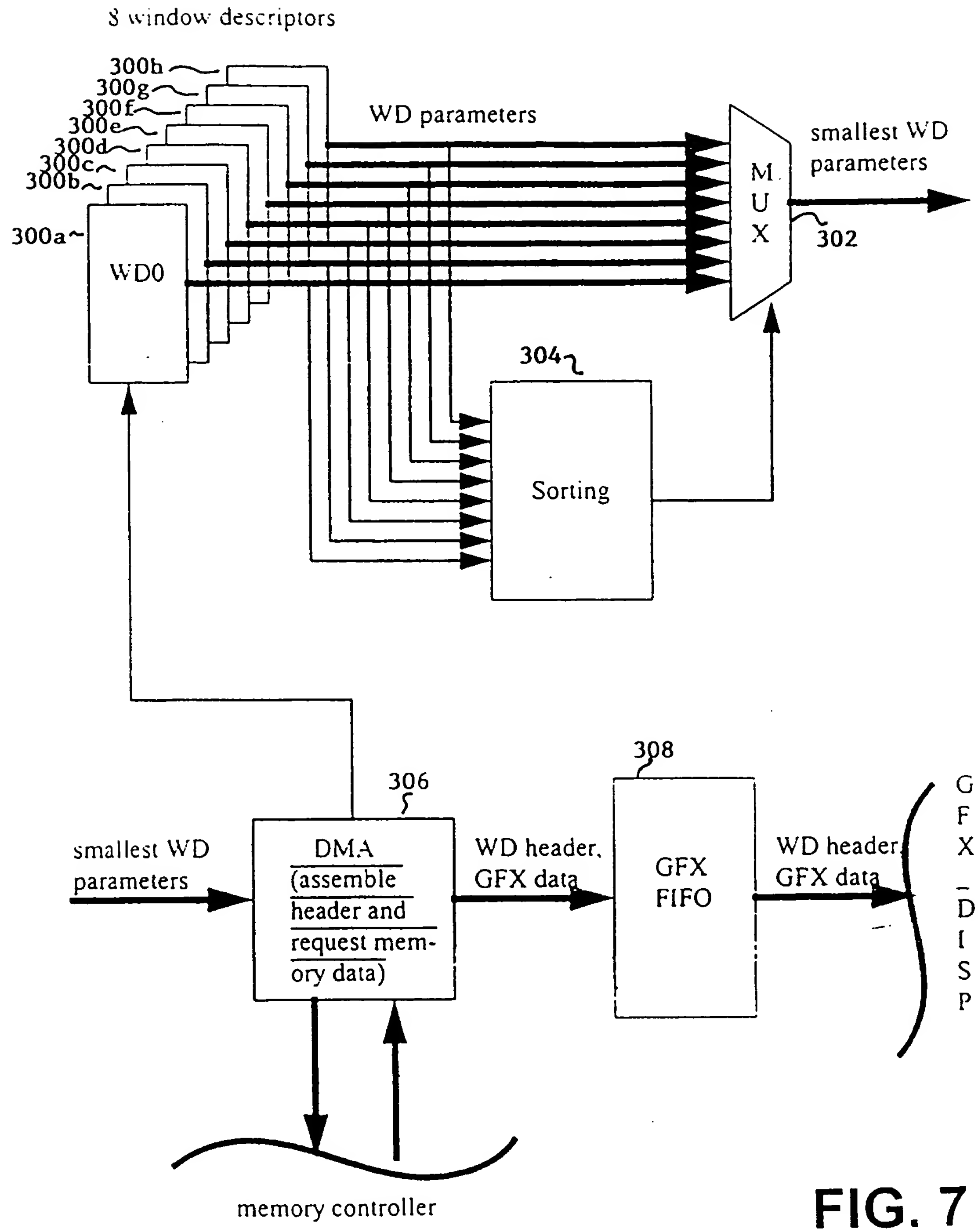

FIG. 7

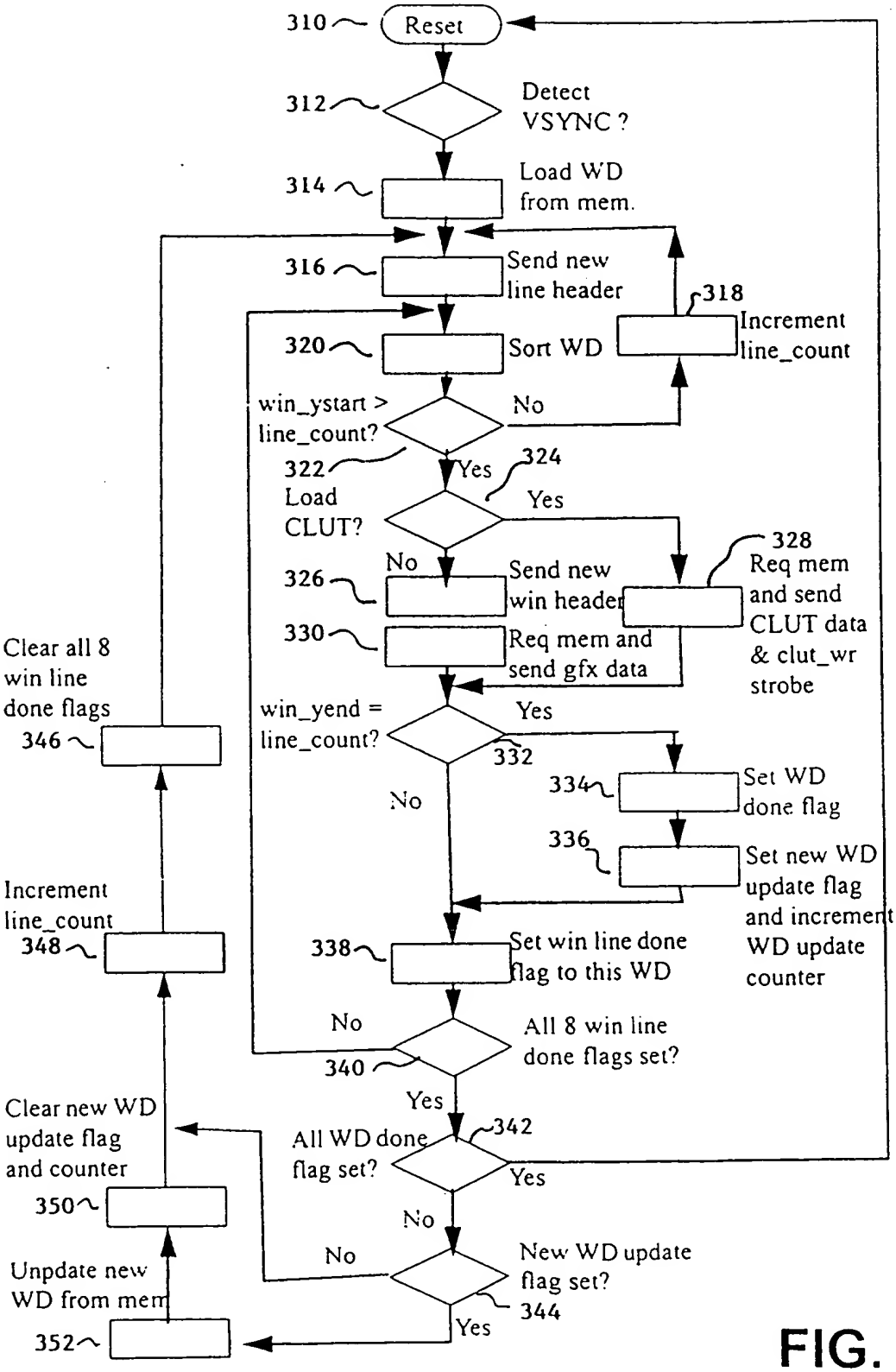
310
Reset
312
Detect VSYNC ?
314
Load WD from mem.
316
Send new line header
318
Increment line_count
320
Sort WD
win_ystart > line_count?
No
Yes
322
Load CLUT?
324
Yes
No
326
Send new win header
328
Req mem and send CLUT data & clut_wr strobe
330
Req mem and send gfx data
win_yend = line_count?
Yes
332
No
334
Set WD done flag
336
Set new WD update flag and increment WD update counter
338
Set win line done flag to this WD
No
340
All 8 win line done flags set?
Yes
342
All WD done flag set?
Yes
No
No
New WD update flag set?
344
Yes
352
Unpdate new WD from mem
350
Clear new WD update flag and counter
348
Increment line_count
346
Clear all 8 win line done flags

FIG. 8

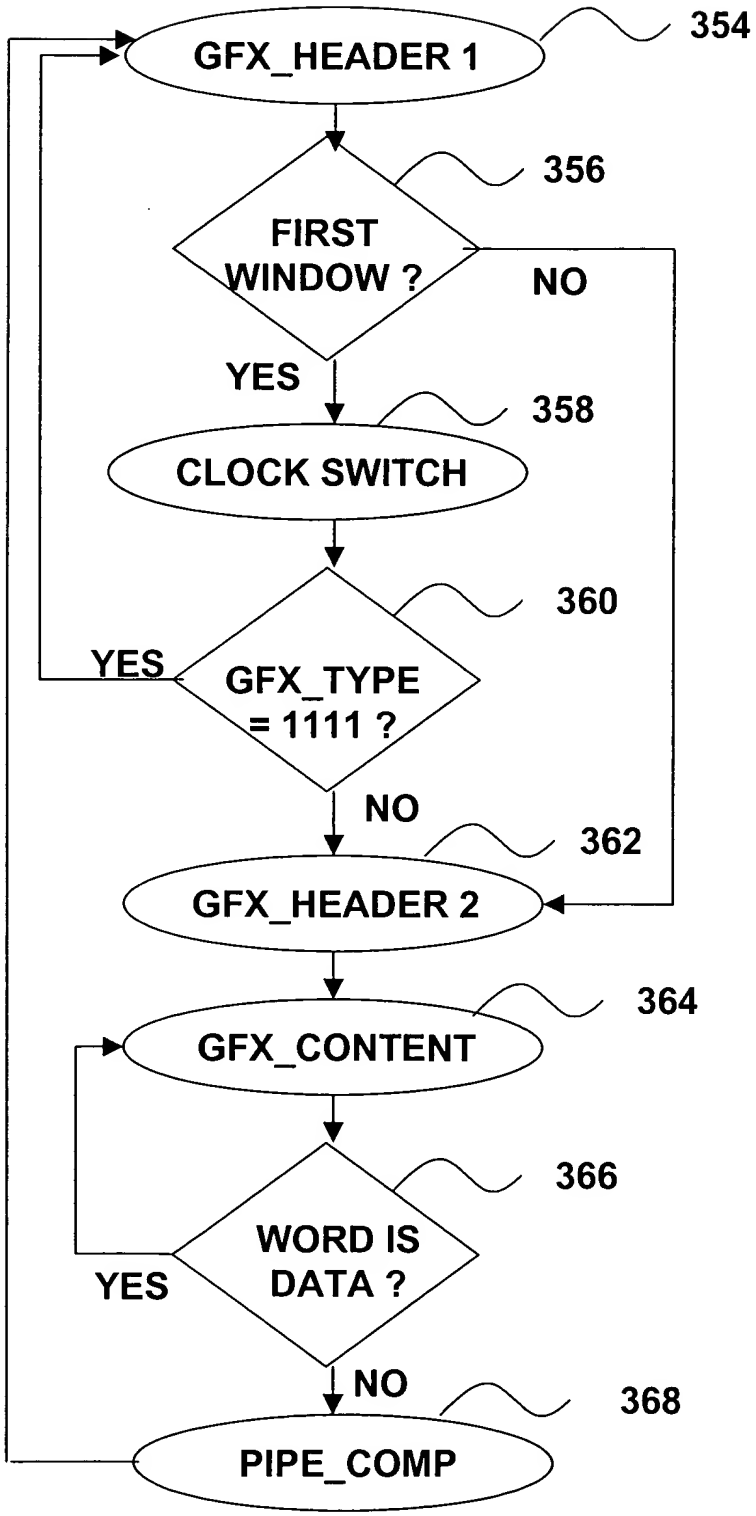
GFX_HEADER 1
354
356
FIRST WINDOW ?
NO
YES
358
CLOCK SWITCH
360
YES
GFX_TYPE = 1111 ?
NO
362
GFX_HEADER 2
364
GFX_CONTENT
366
WORD IS DATA ?
YES
NO
368
PIPE_COMP

FIG. 9

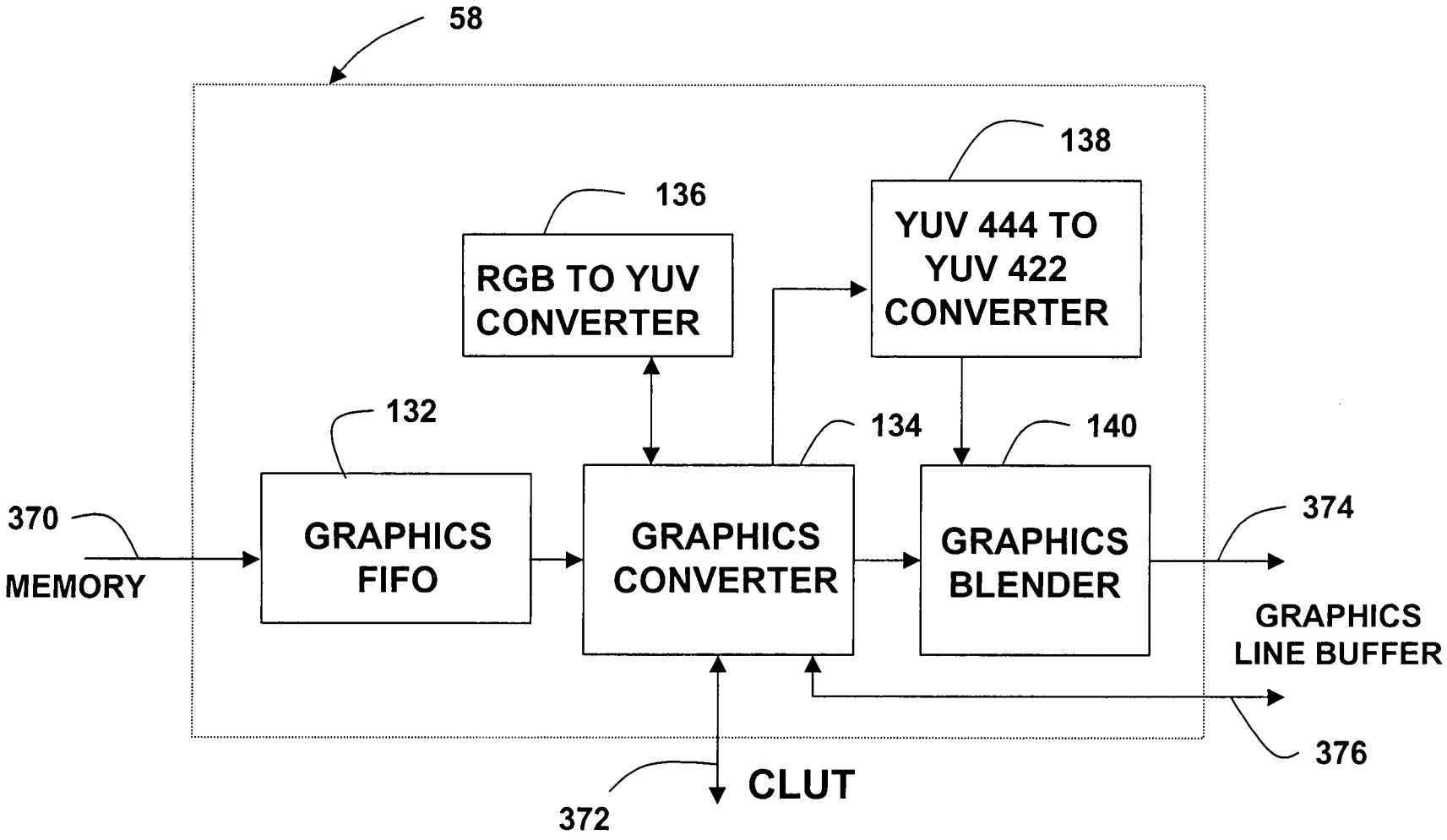

FIG. 10

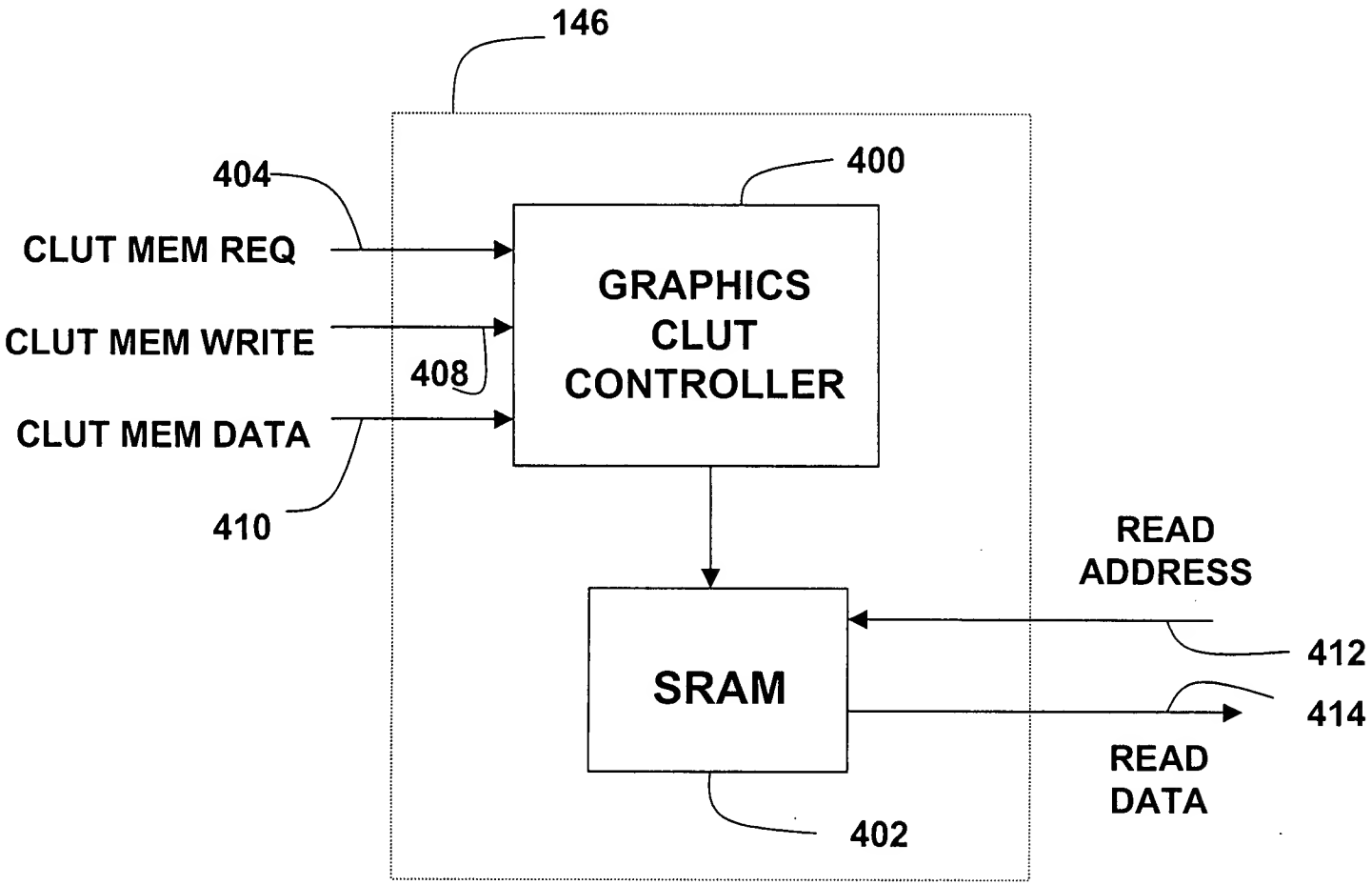
146
404
400
CLUT MEM REQ
CLUT MEM WRITE
408
CLUT MEM DATA
410
GRAPHICS CLUT CONTROLLER
READ ADDRESS
412
SRAM
414
READ DATA
402

FIG. 11

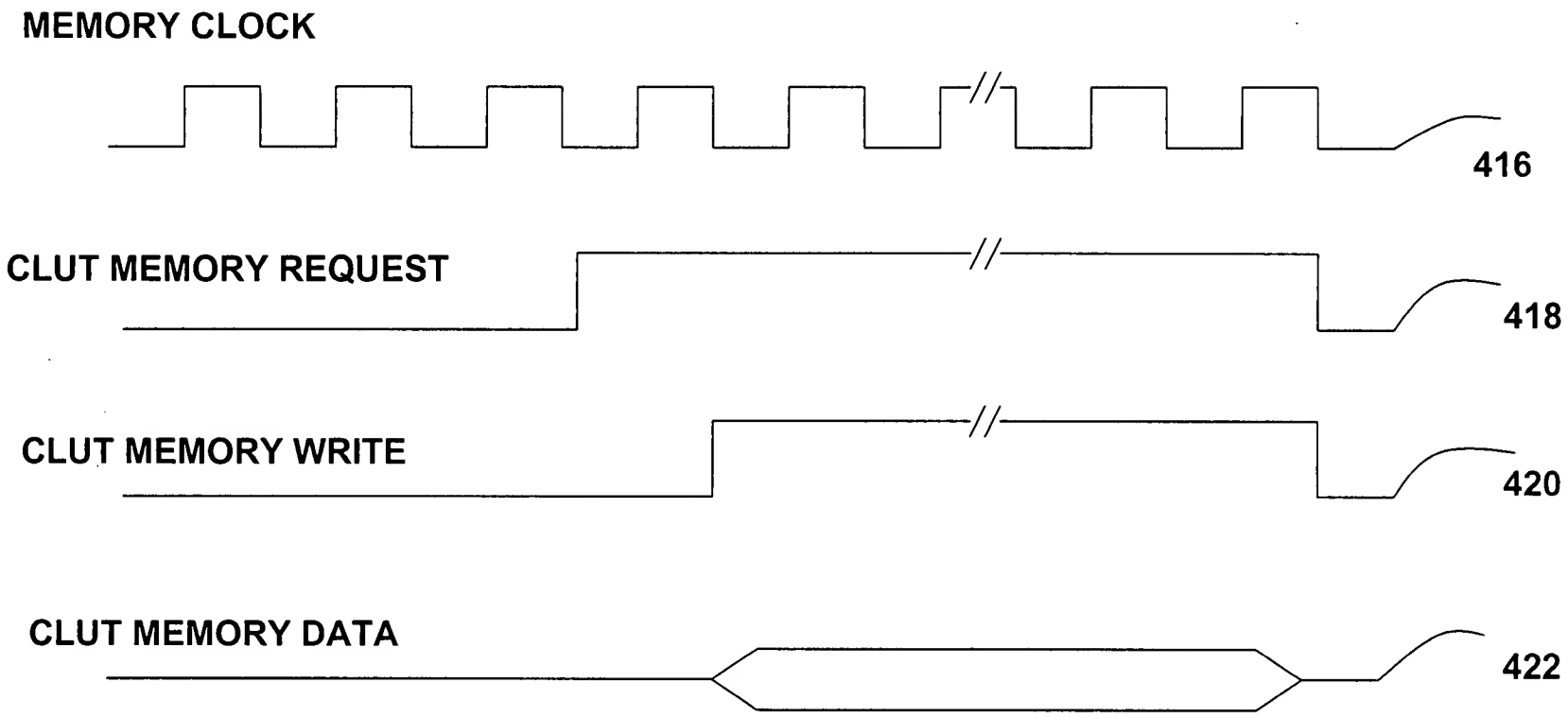

FIG. 12

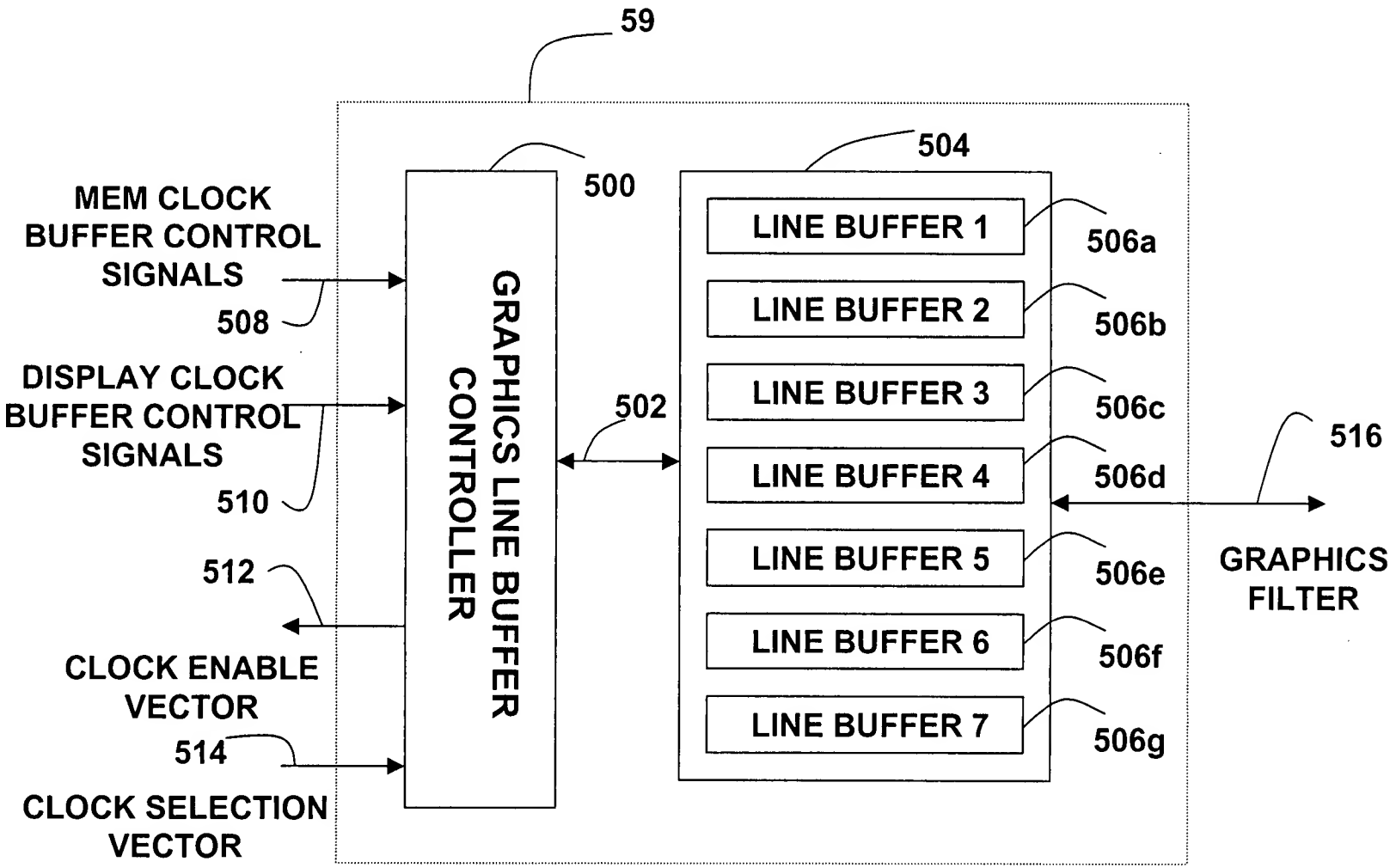

FIG. 13

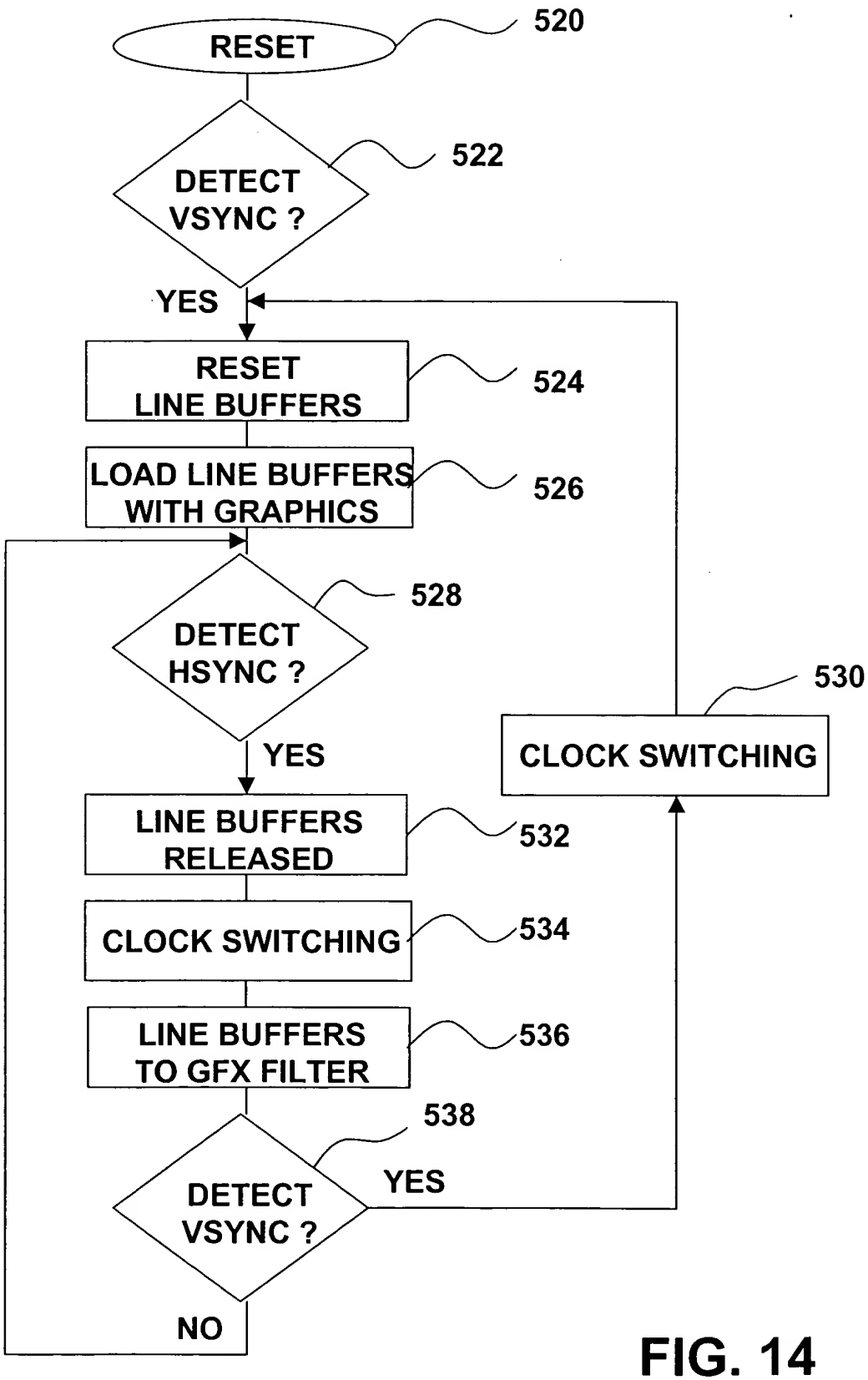
RESET
520
DETECT VSYNC ?
522
YES
RESET LINE BUFFERS
524
LOAD LINE BUFFERS WITH GRAPHICS
526
DETECT HSYNC ?
528
YES
LINE BUFFERS RELEASED
532
CLOCK SWITCHING
534
LINE BUFFERS TO GFX FILTER
536
DETECT VSYNC ?
538
YES
NO
CLOCK SWITCHING
530

FIG. 14

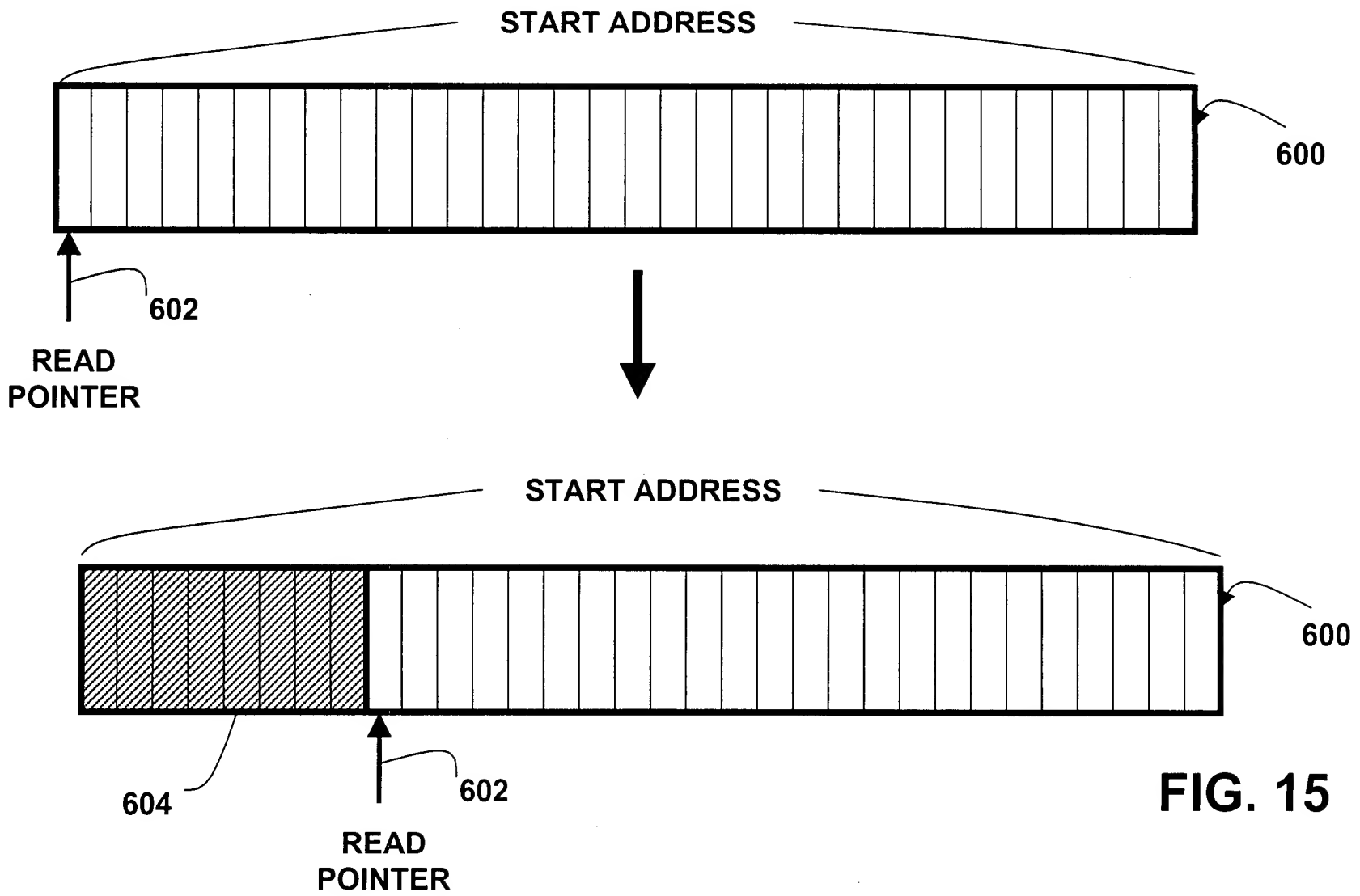

FIG. 15

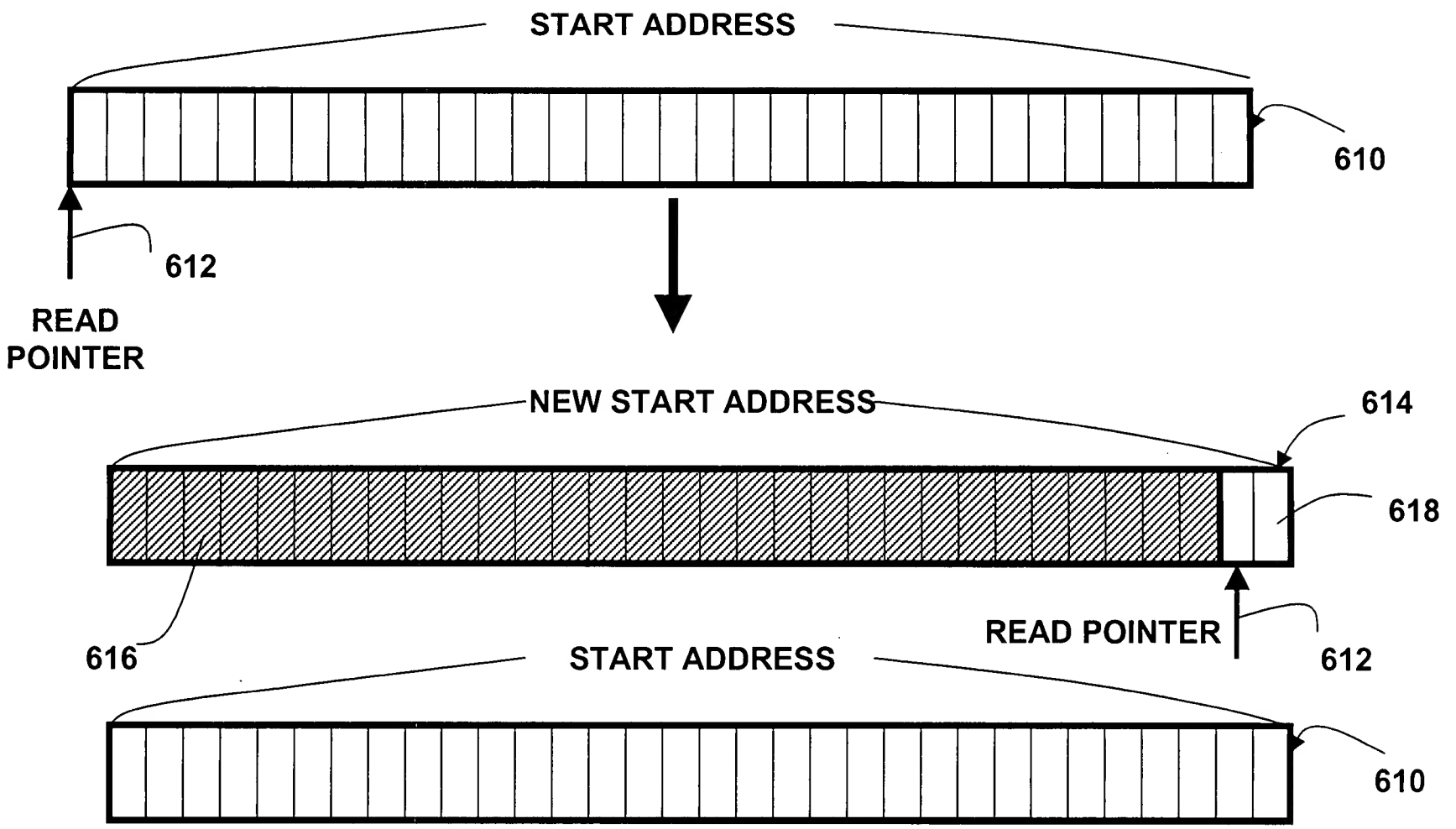

FIG. 16

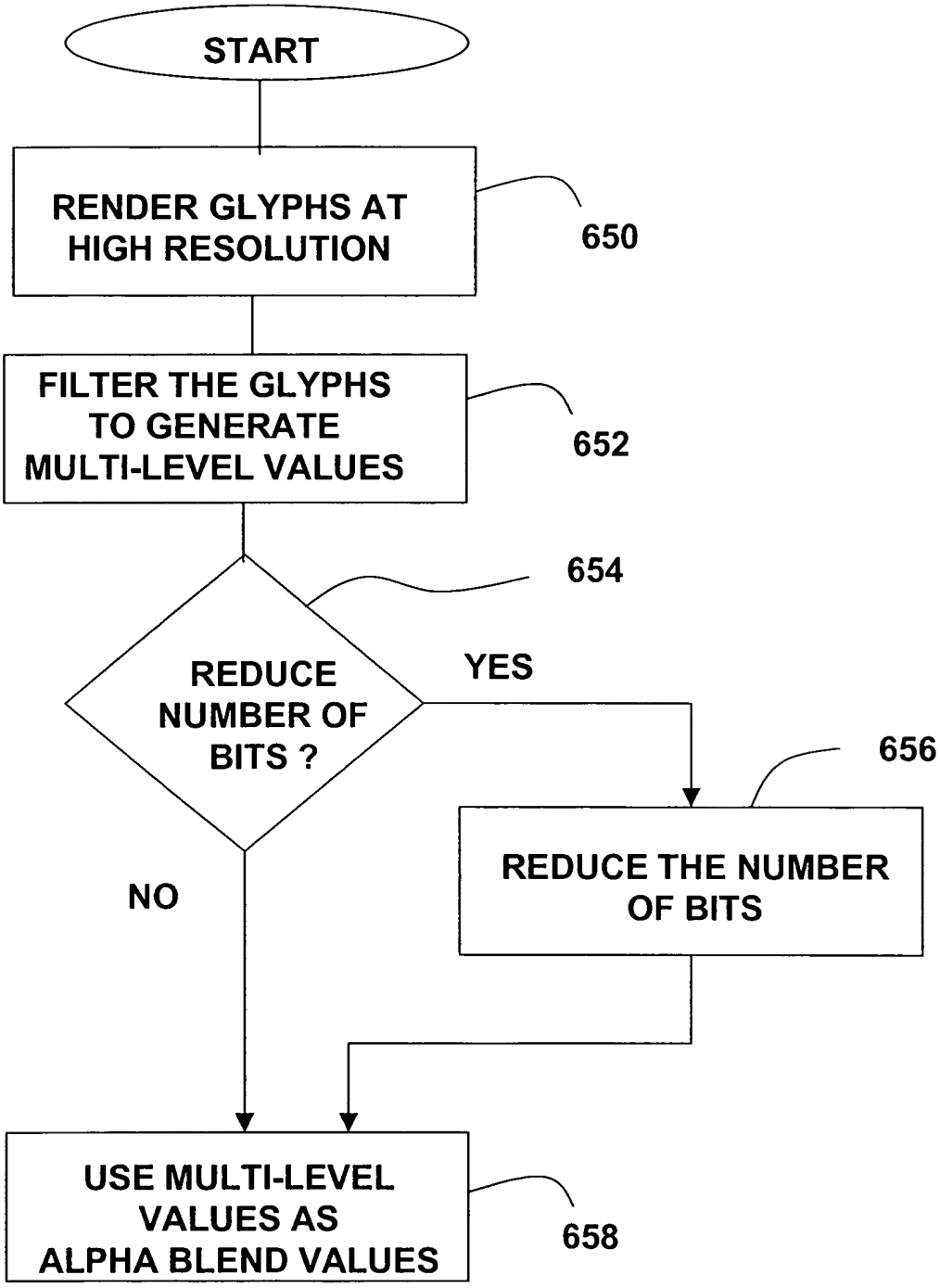

FIG. 17

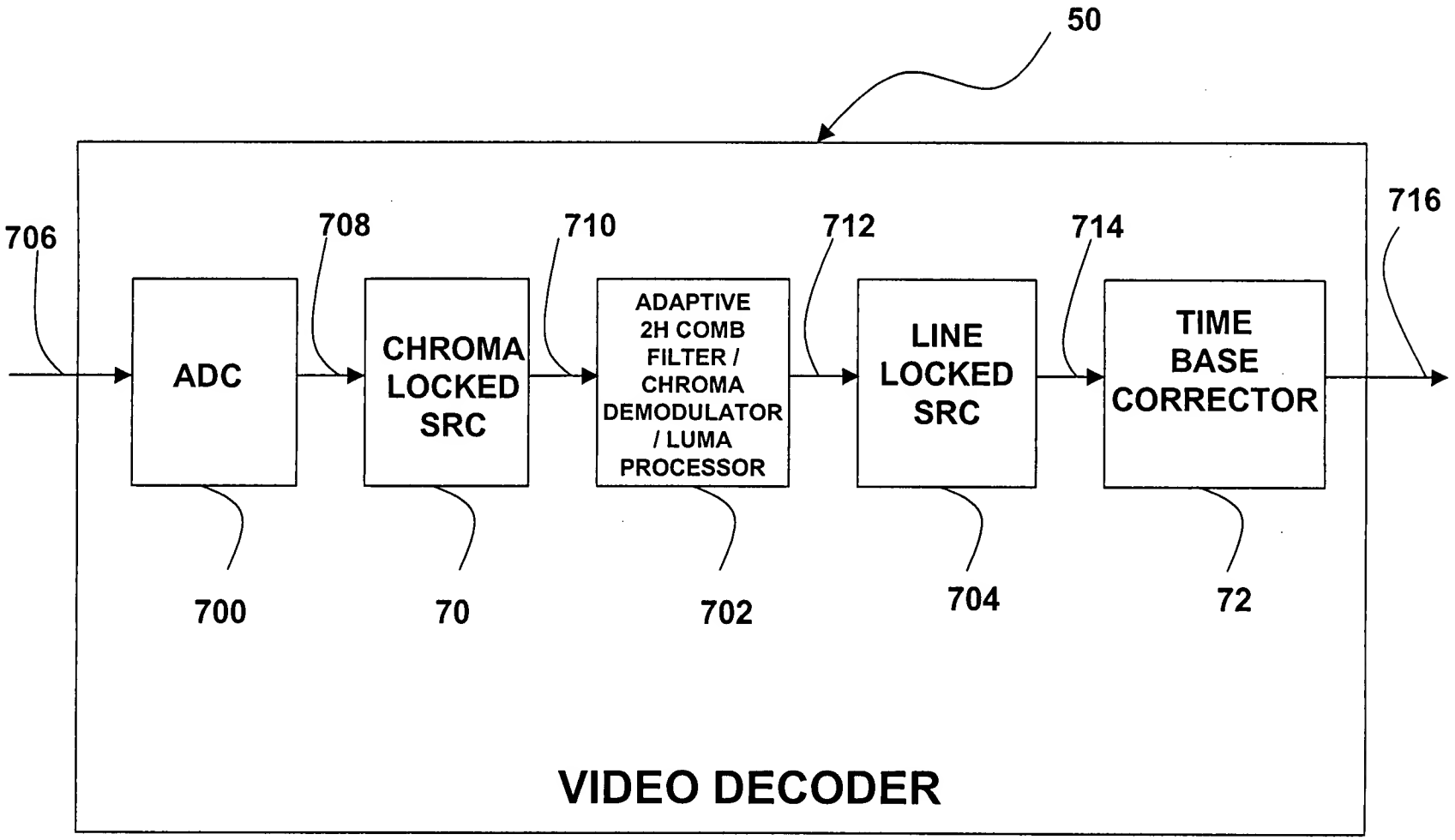

FIG. 18

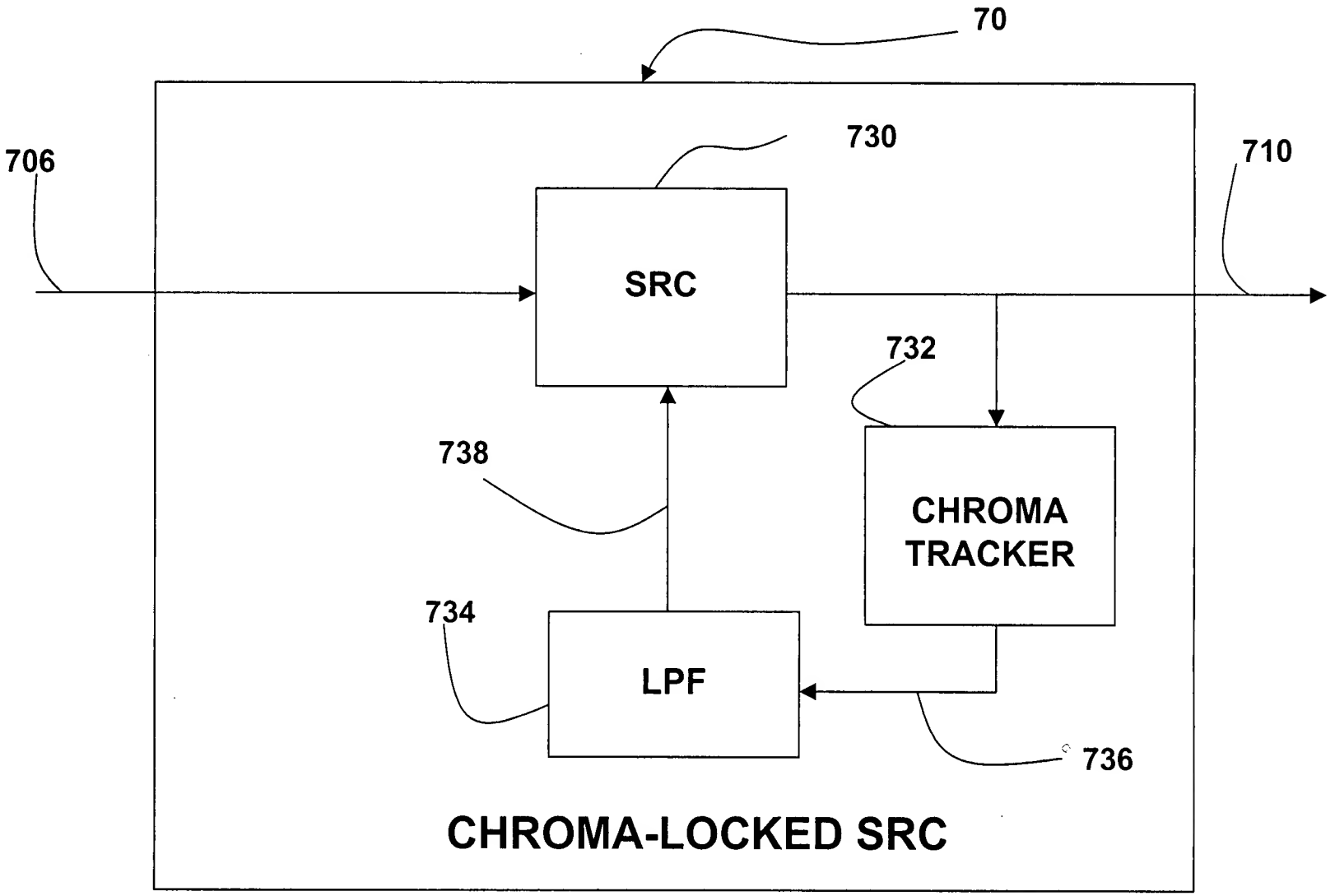

FIG. 19

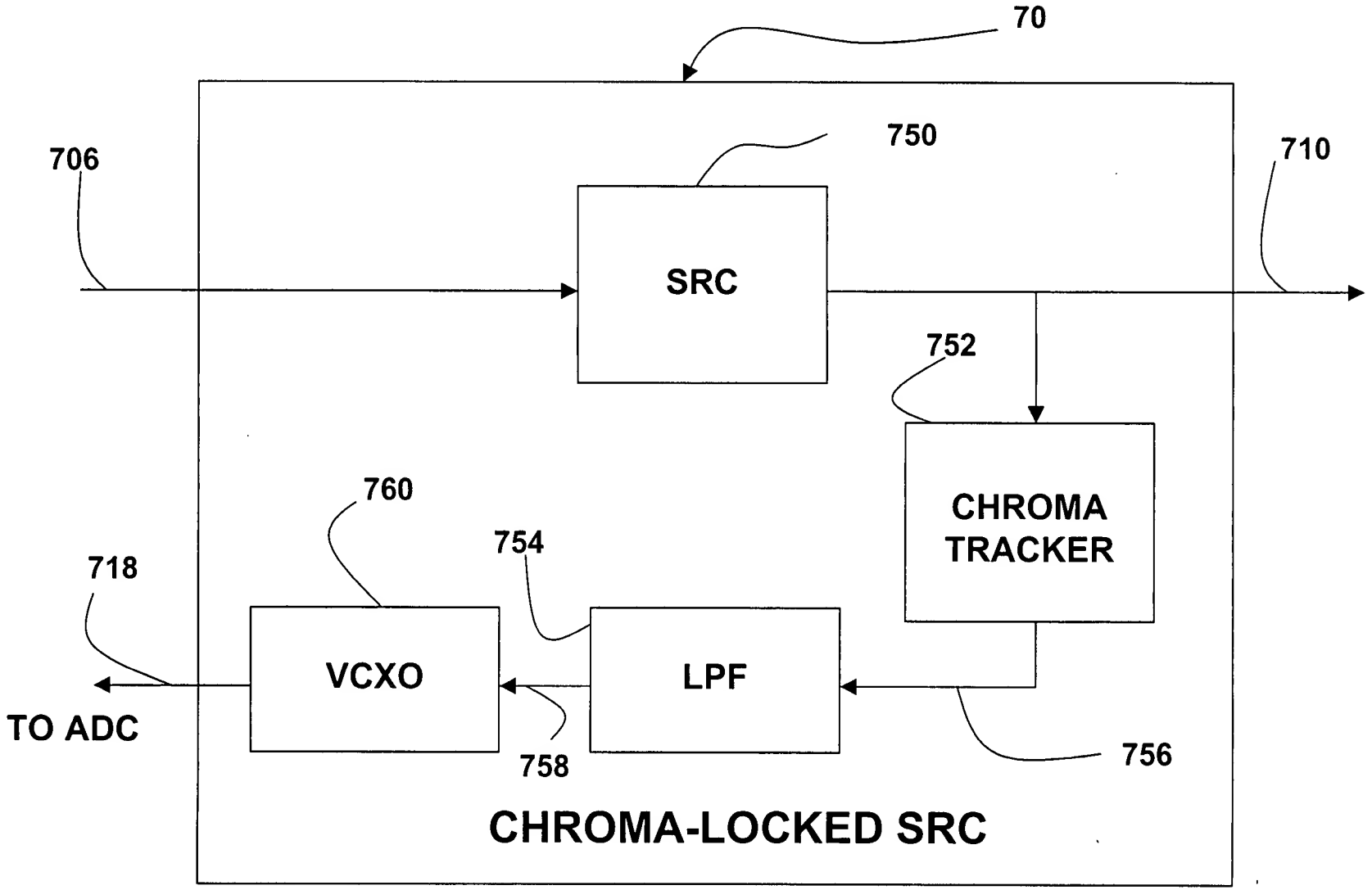

FIG. 20

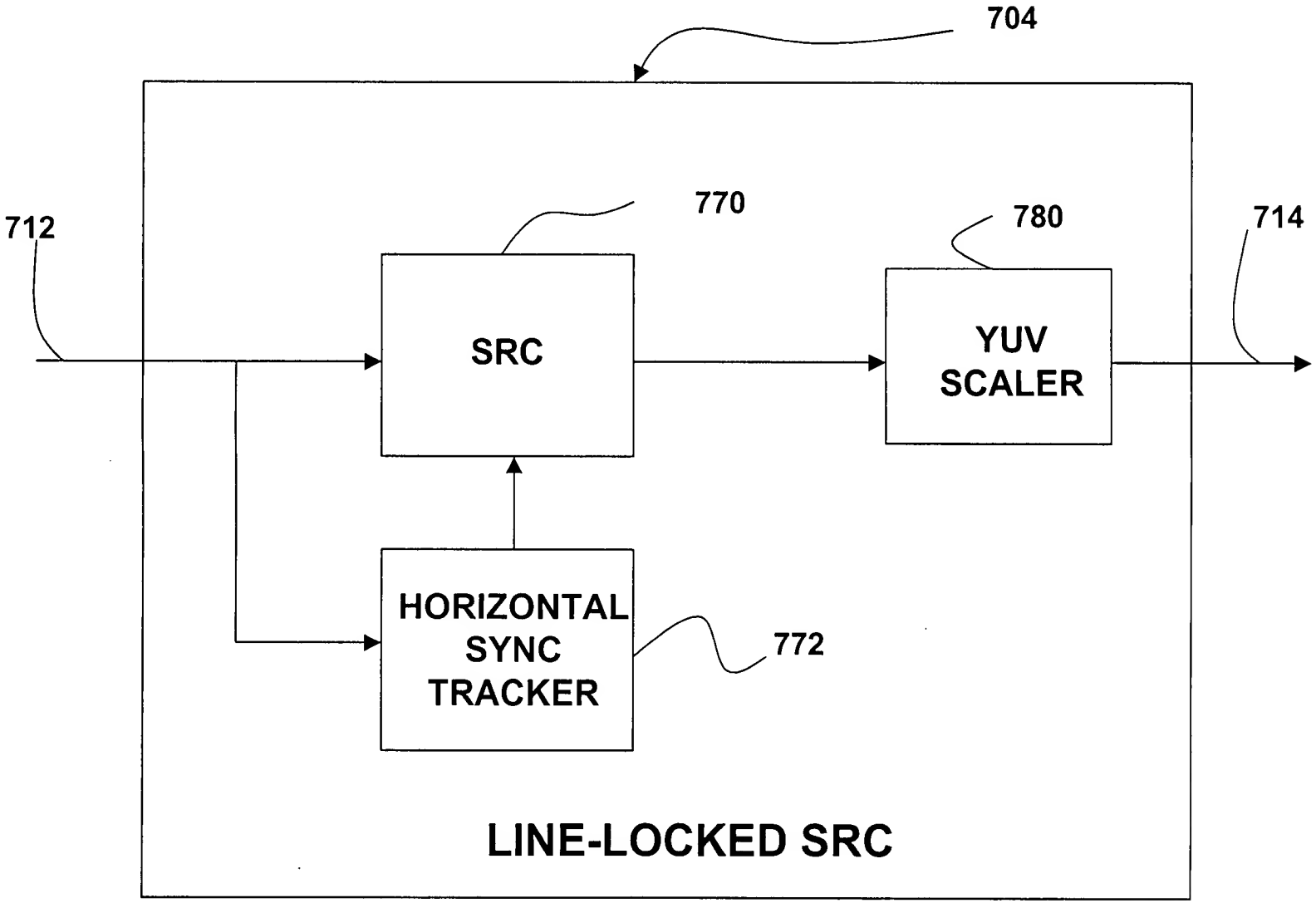

FIG. 21

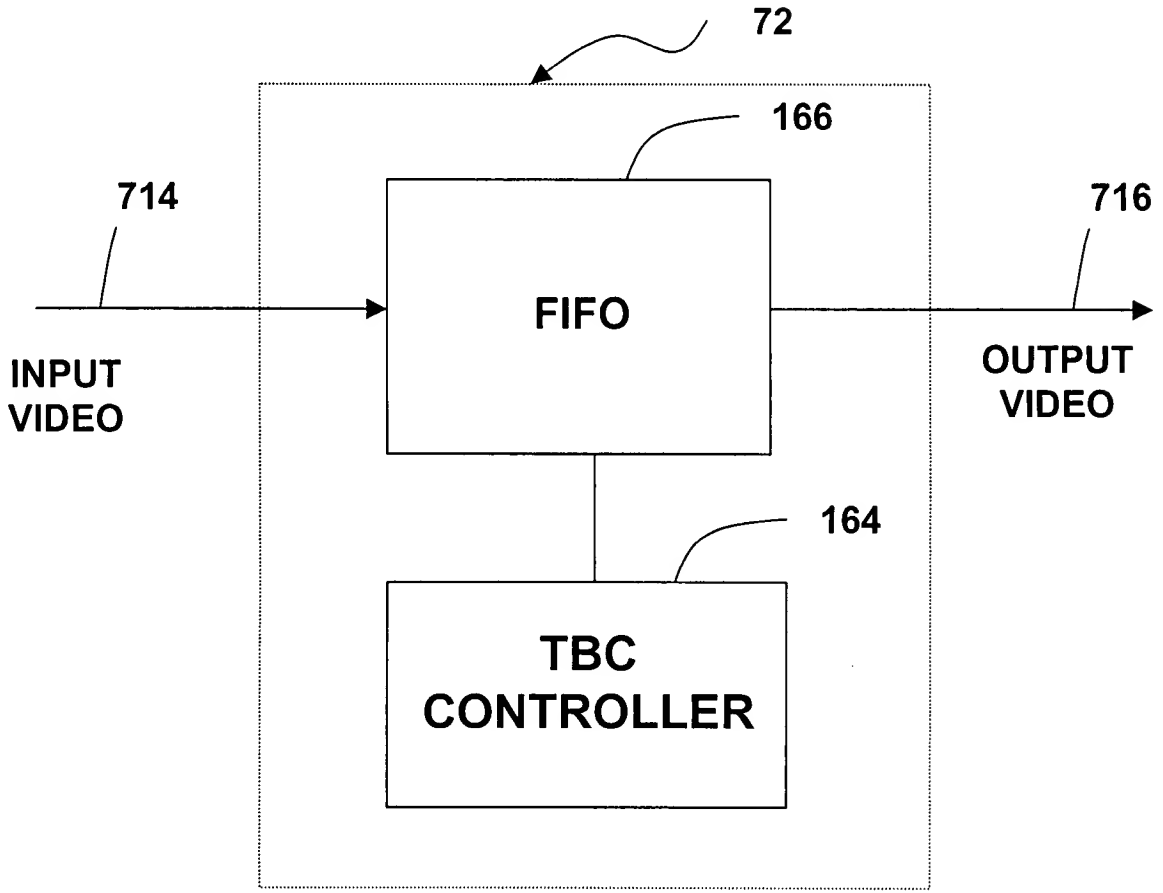

FIG. 22

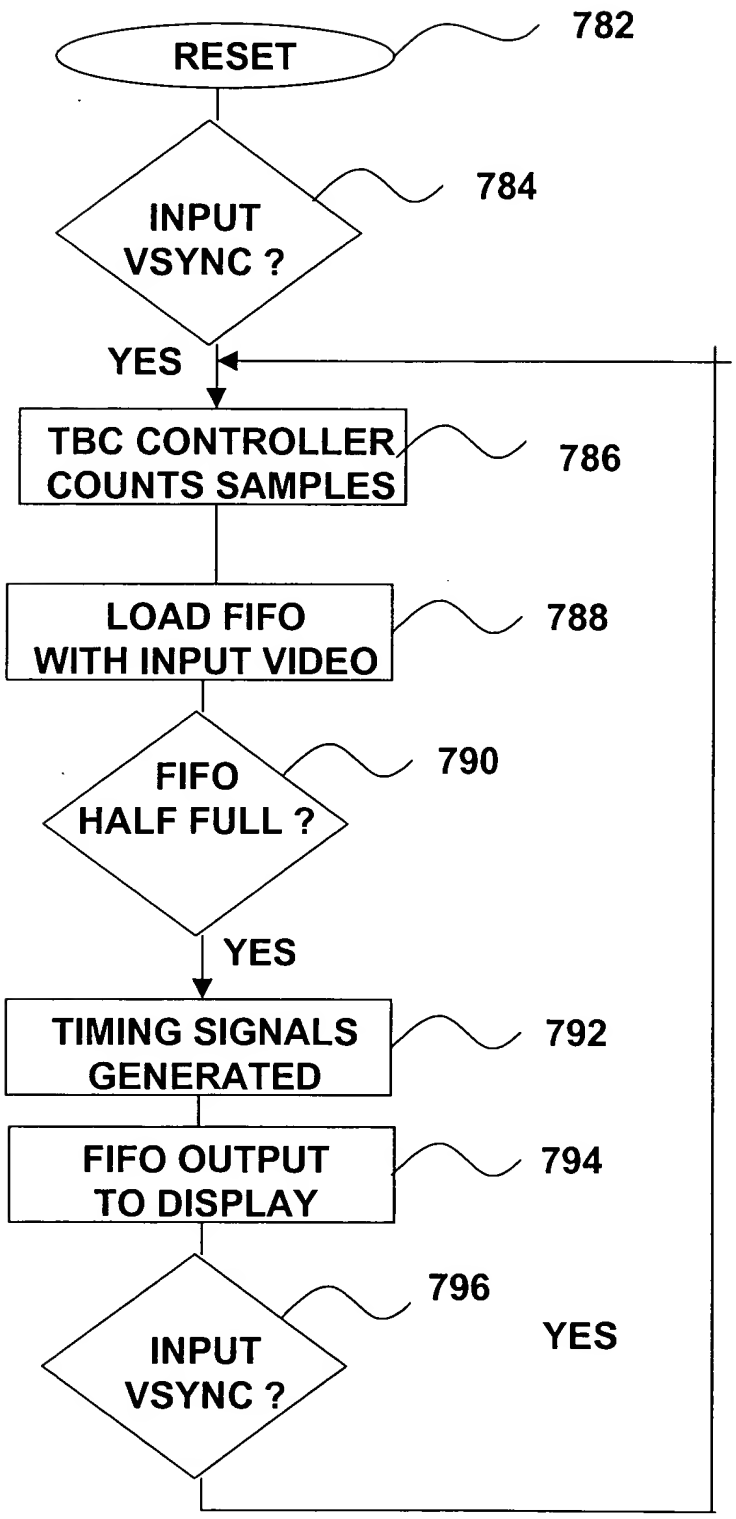
RESET
782
INPUT VSYNC ?
784
YES
TBC CONTROLLER COUNTS SAMPLES
786
LOAD FIFO WITH INPUT VIDEO
788
FIFO HALF FULL ?
790
YES
TIMING SIGNALS GENERATED
792
FIFO OUTPUT TO DISPLAY
794
INPUT VSYNC ?
796
YES

FIG. 23

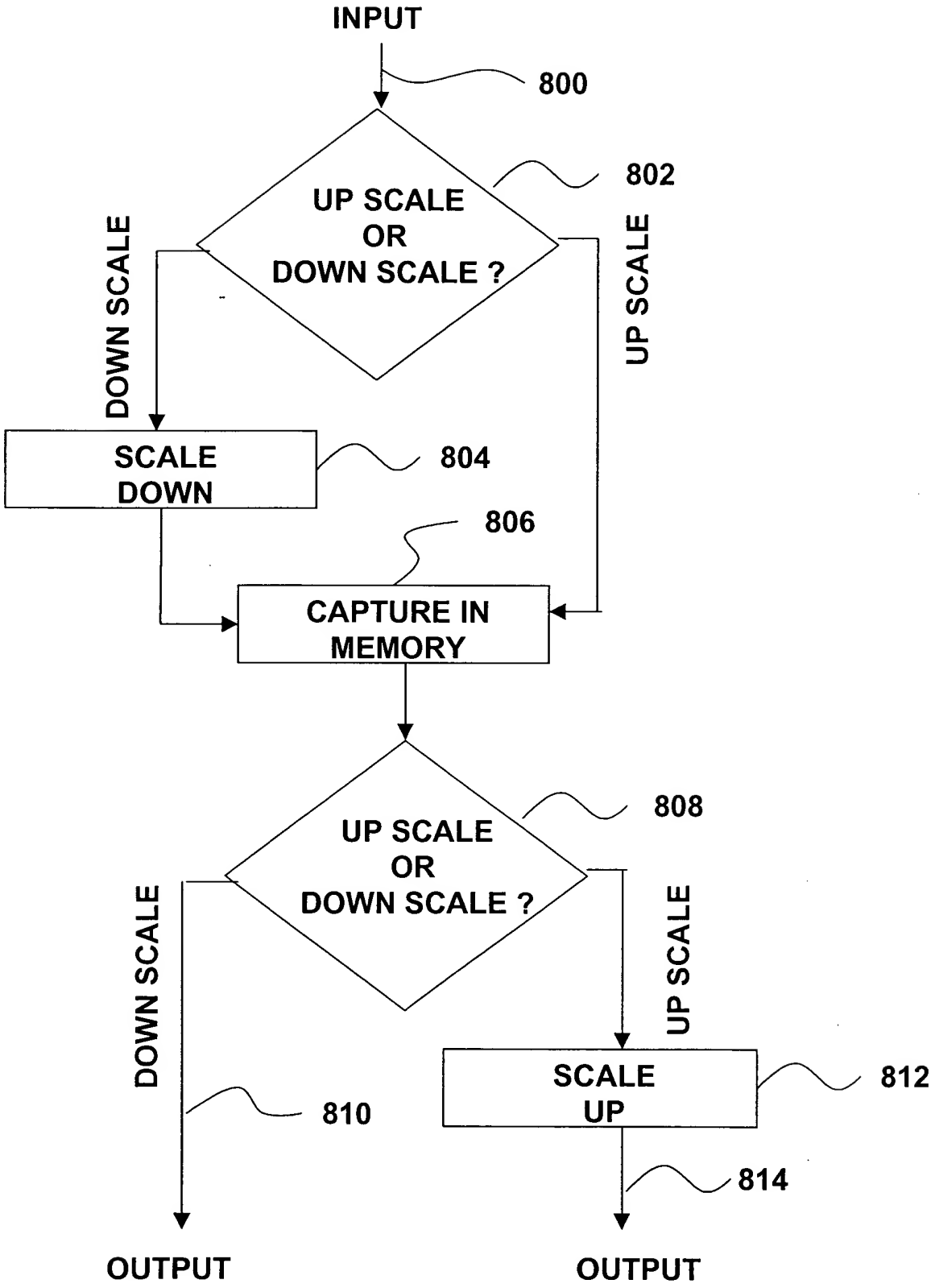
INPUT
800
UP SCALE OR DOWN SCALE ?
802
DOWN SCALE
UP SCALE
SCALE DOWN
804
806
CAPTURE IN MEMORY
UP SCALE OR DOWN SCALE ?
808
DOWN SCALE
UP SCALE
SCALE UP
812
810
814
OUTPUT
OUTPUT

FIG. 24

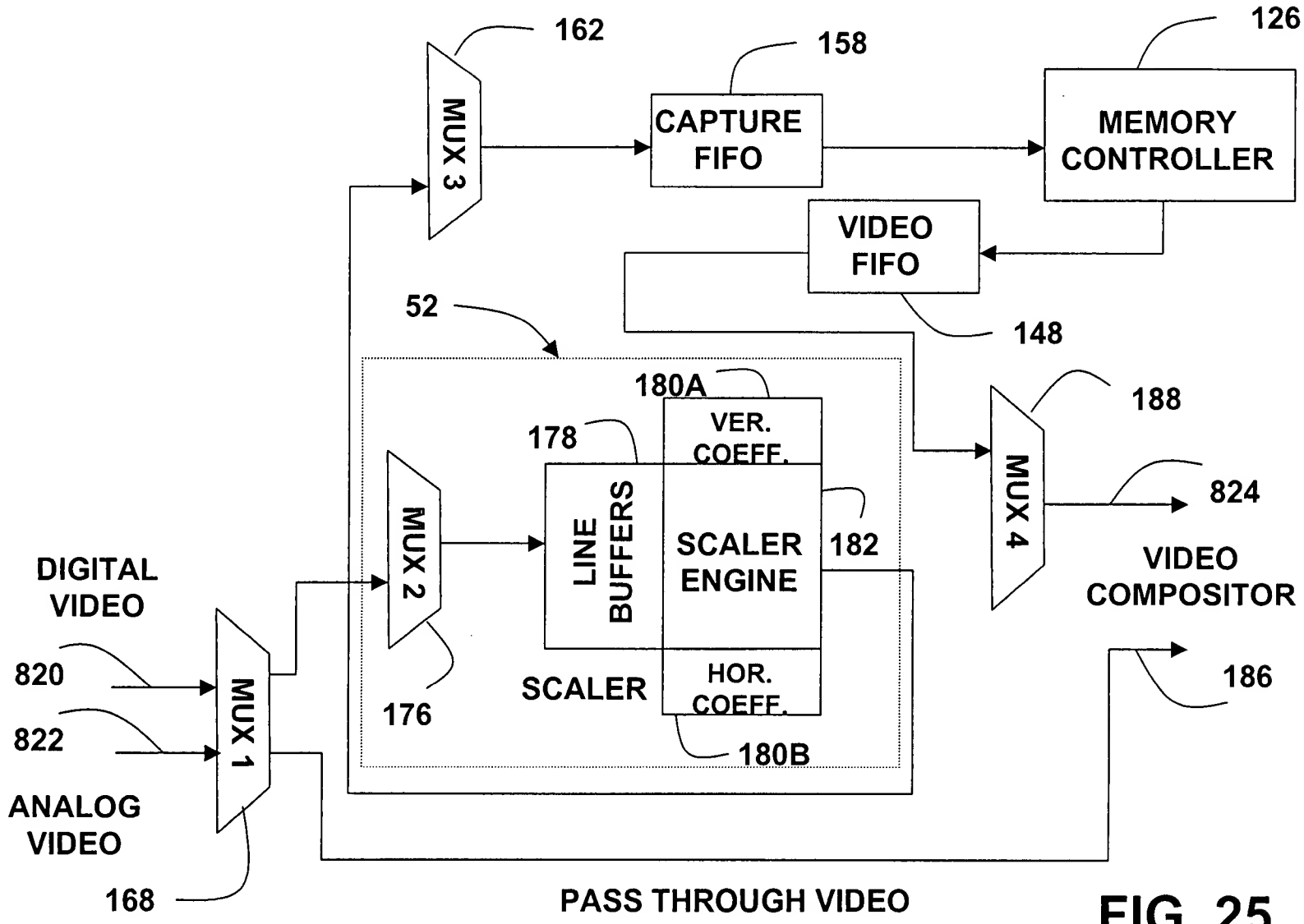

FIG. 25

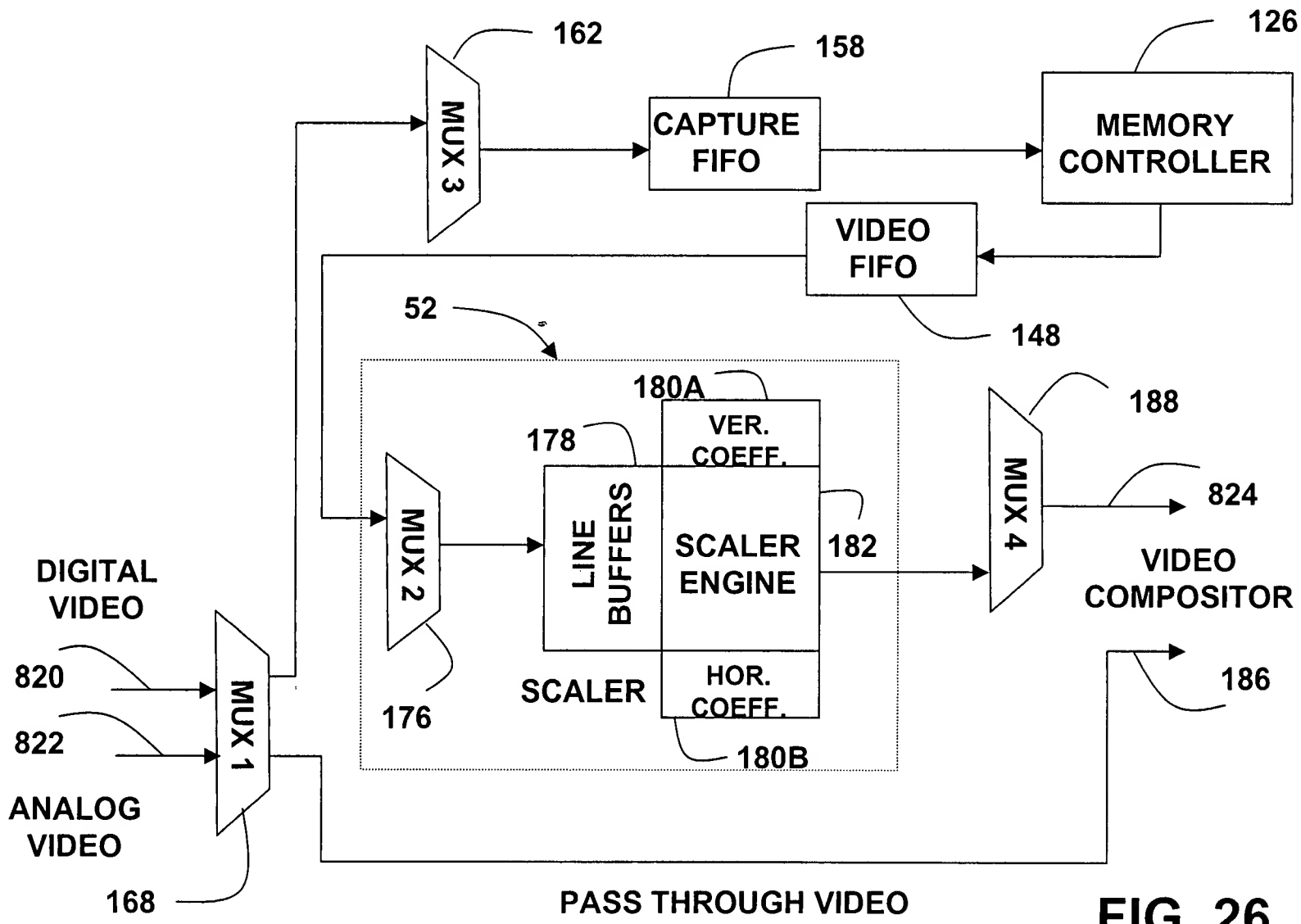

FIG. 26

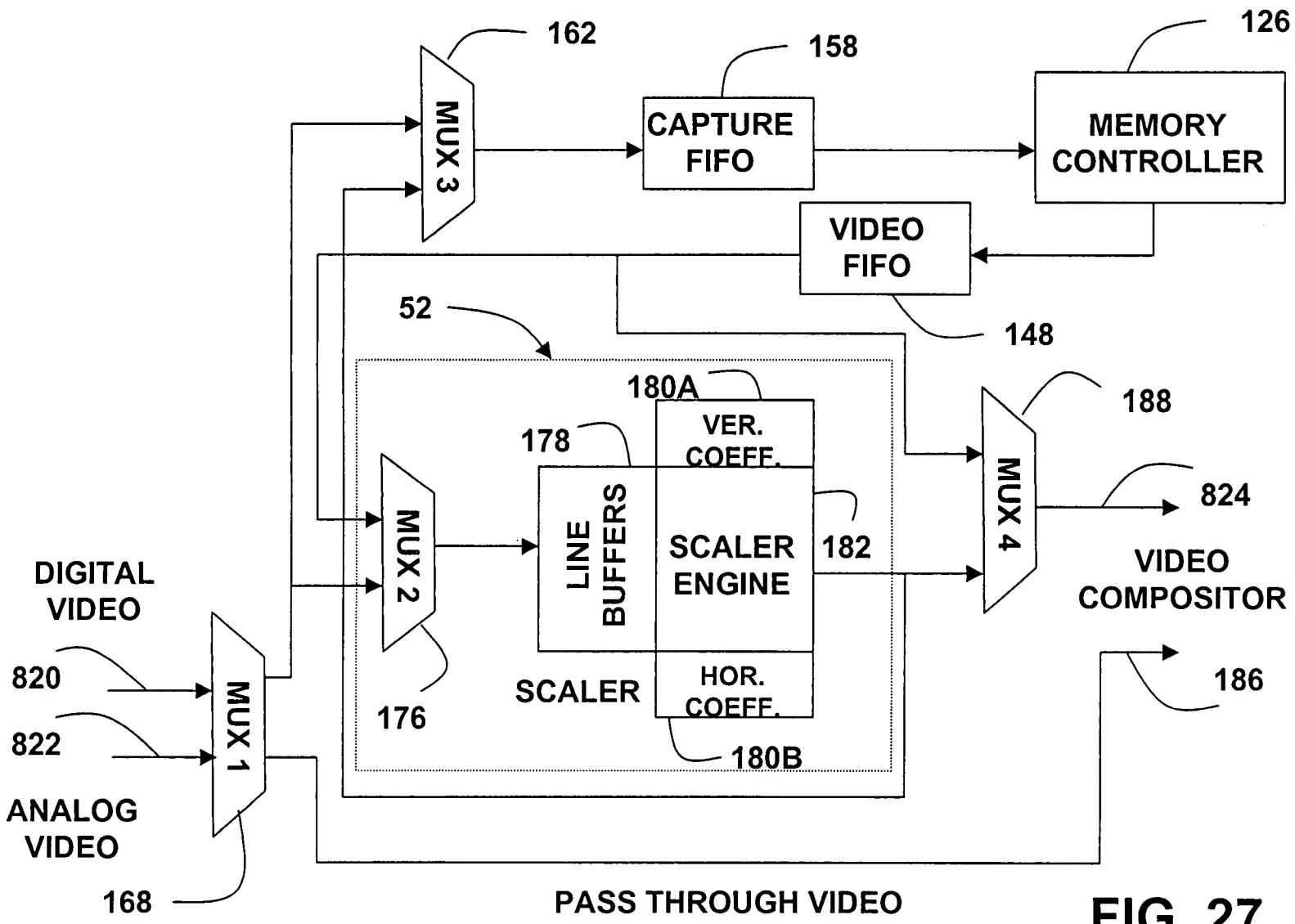

FIG. 27

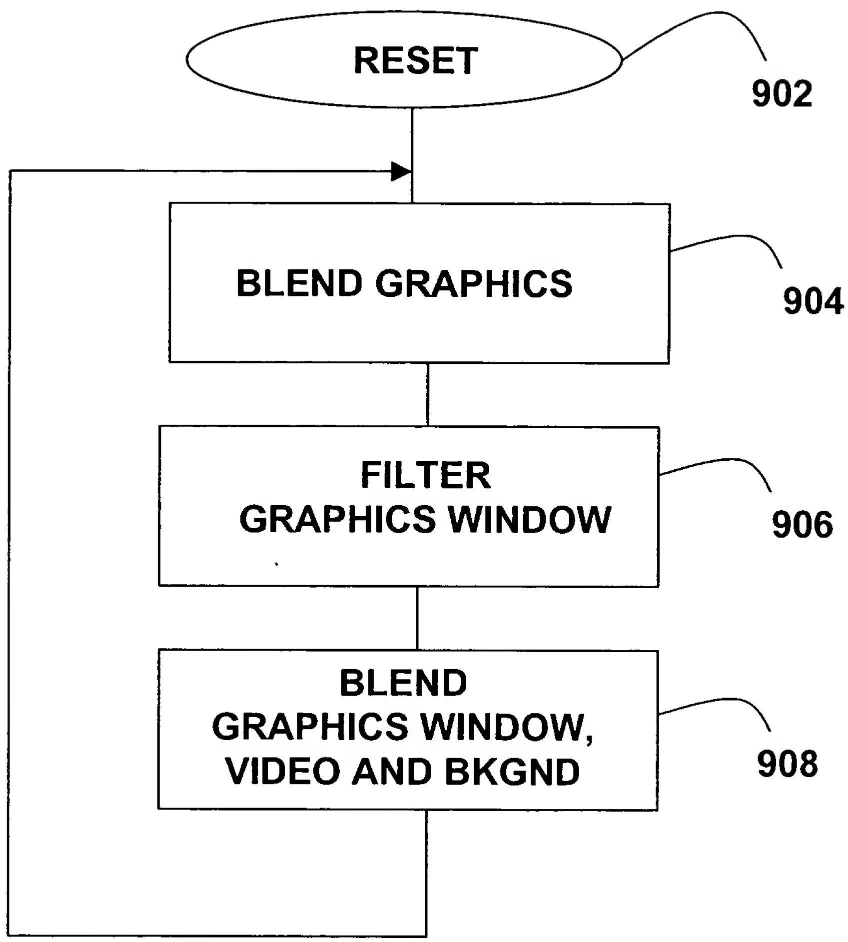
RESET
902
BLEND GRAPHICS
904
FILTER
GRAPHICS WINDOW
906
BLEND
GRAPHICS WINDOW,
VIDEO AND BKGND
908

FIG. 28

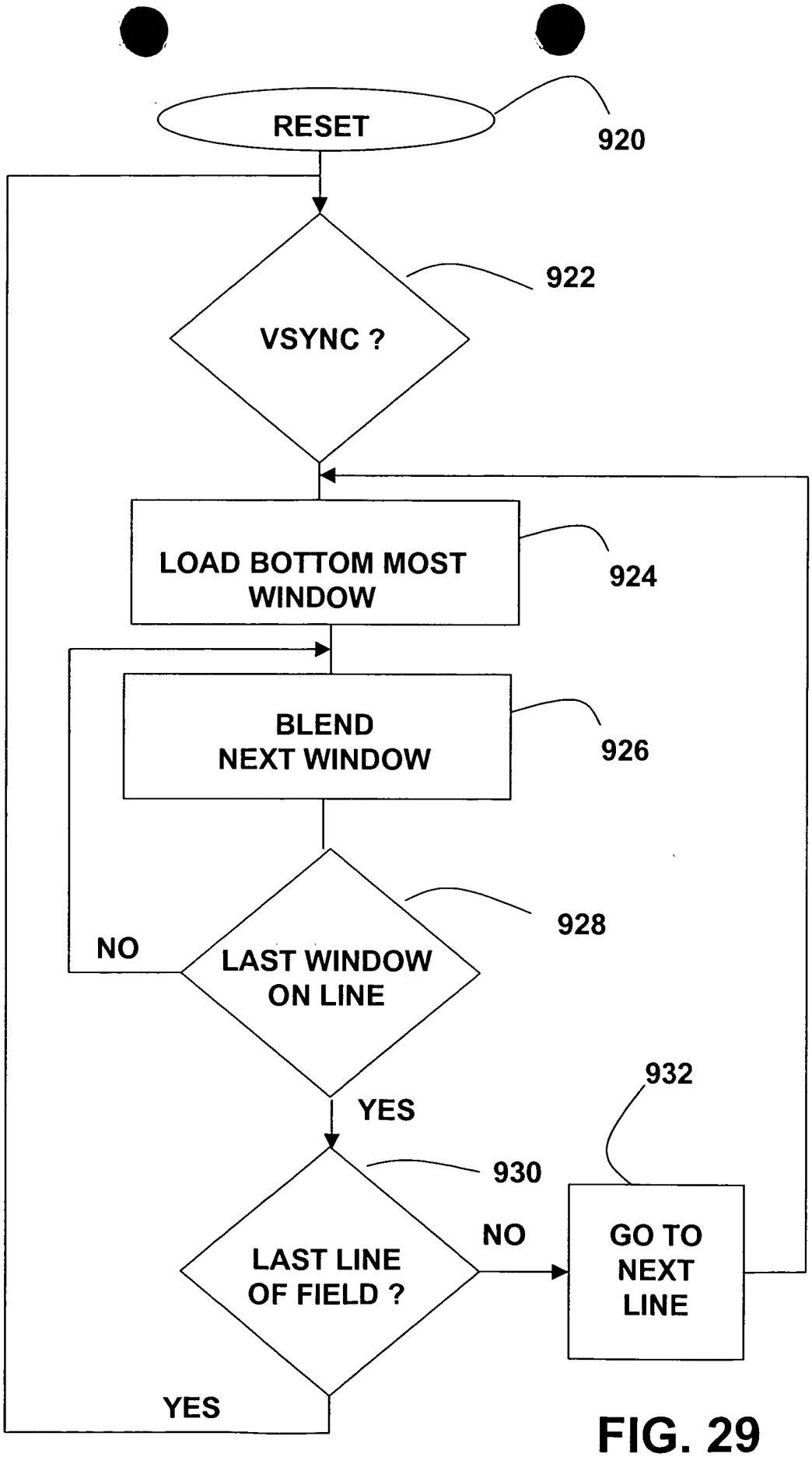

FIG. 29

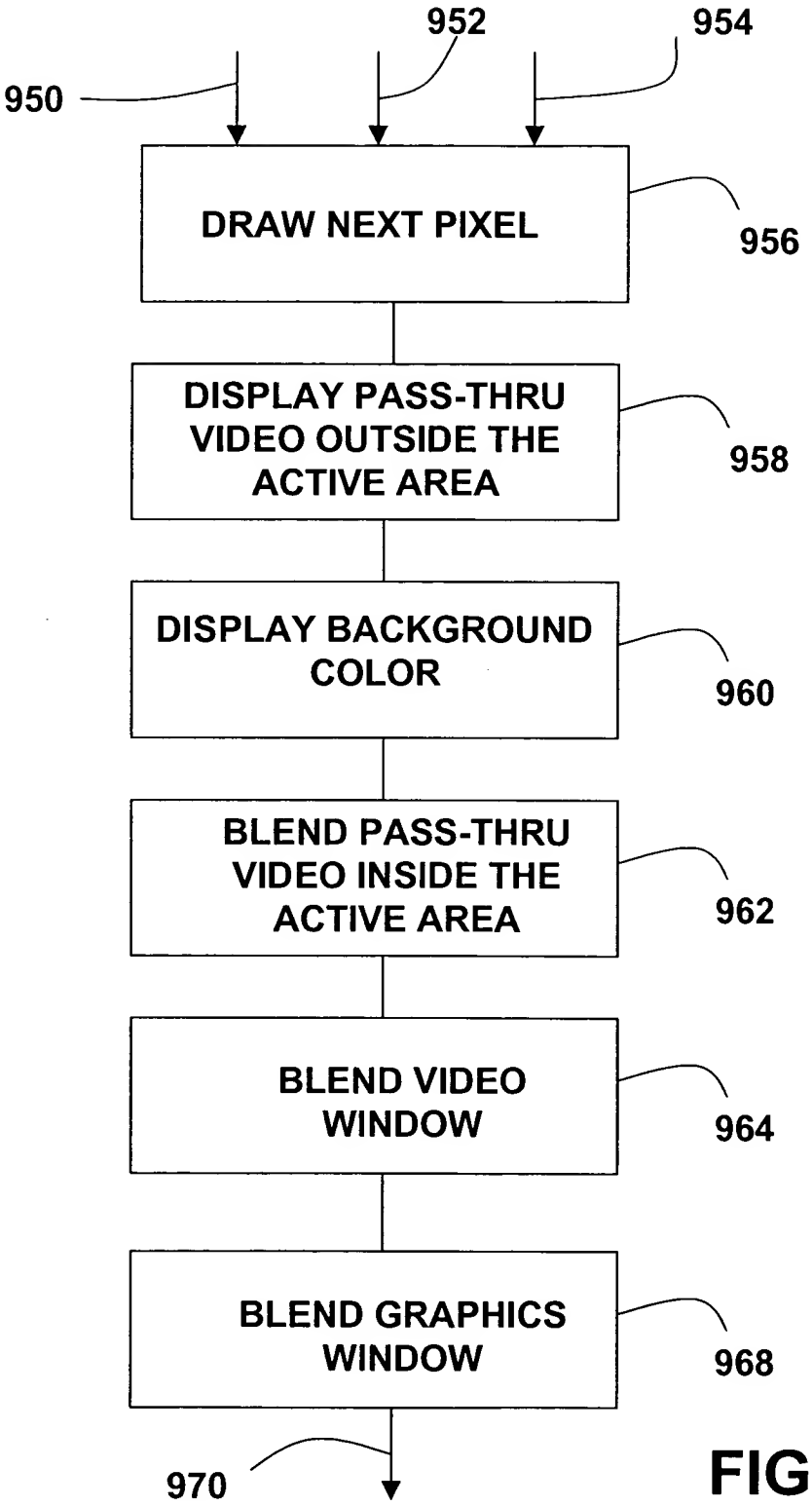
950
952
954
DRAW NEXT PIXEL
956
DISPLAY PASS-THRU VIDEO OUTSIDE THE ACTIVE AREA
958
DISPLAY BACKGROUND COLOR
960
BLEND PASS-THRU VIDEO INSIDE THE ACTIVE AREA
962
BLEND VIDEO WINDOW
964
BLEND GRAPHICS WINDOW
968
970

FIG. 30

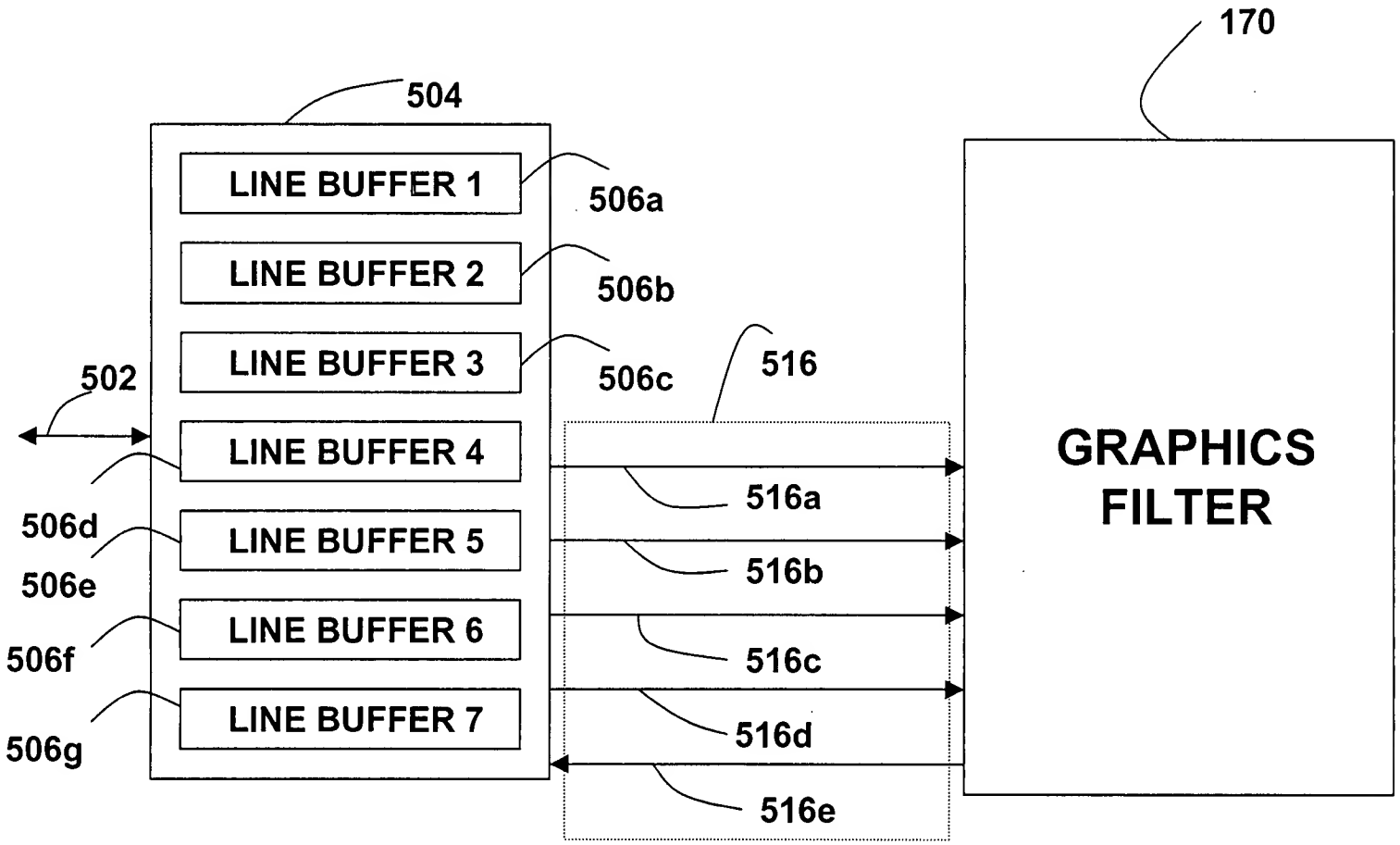

FIG. 31

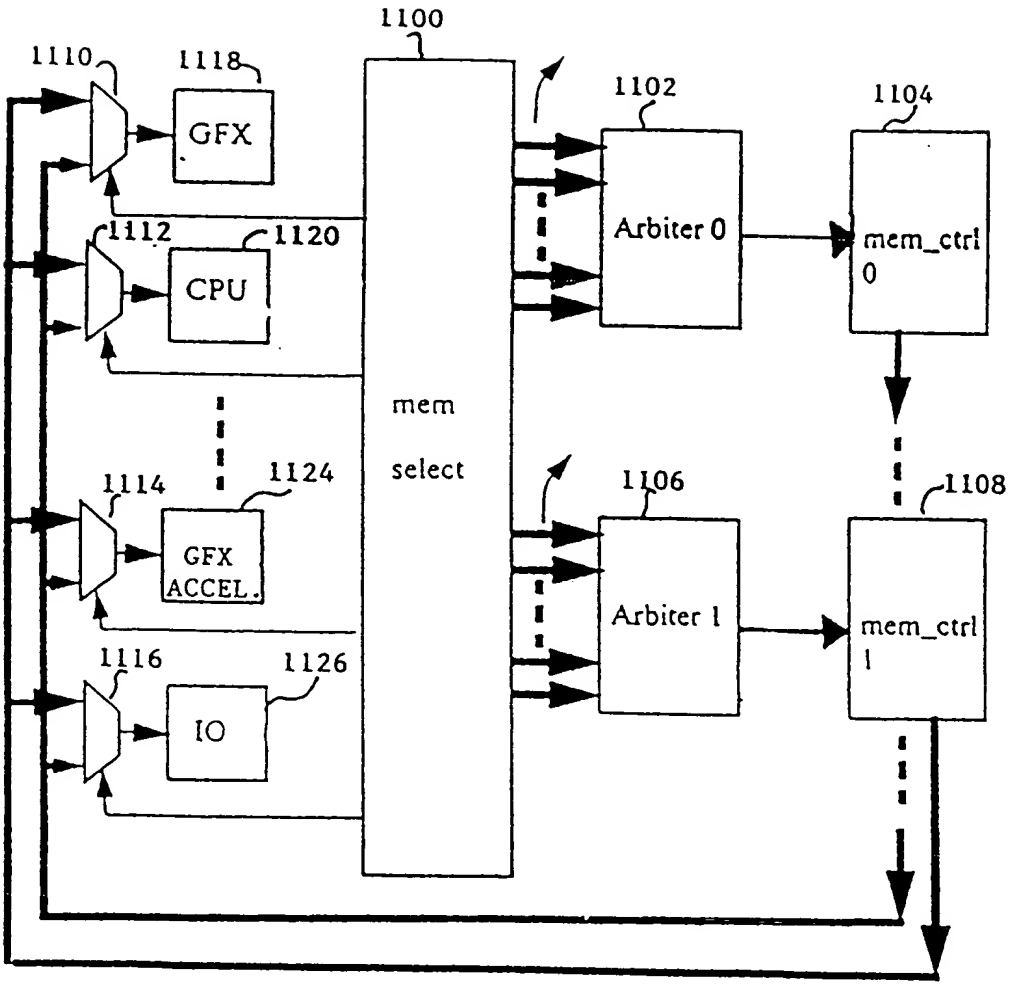

FIG. 32

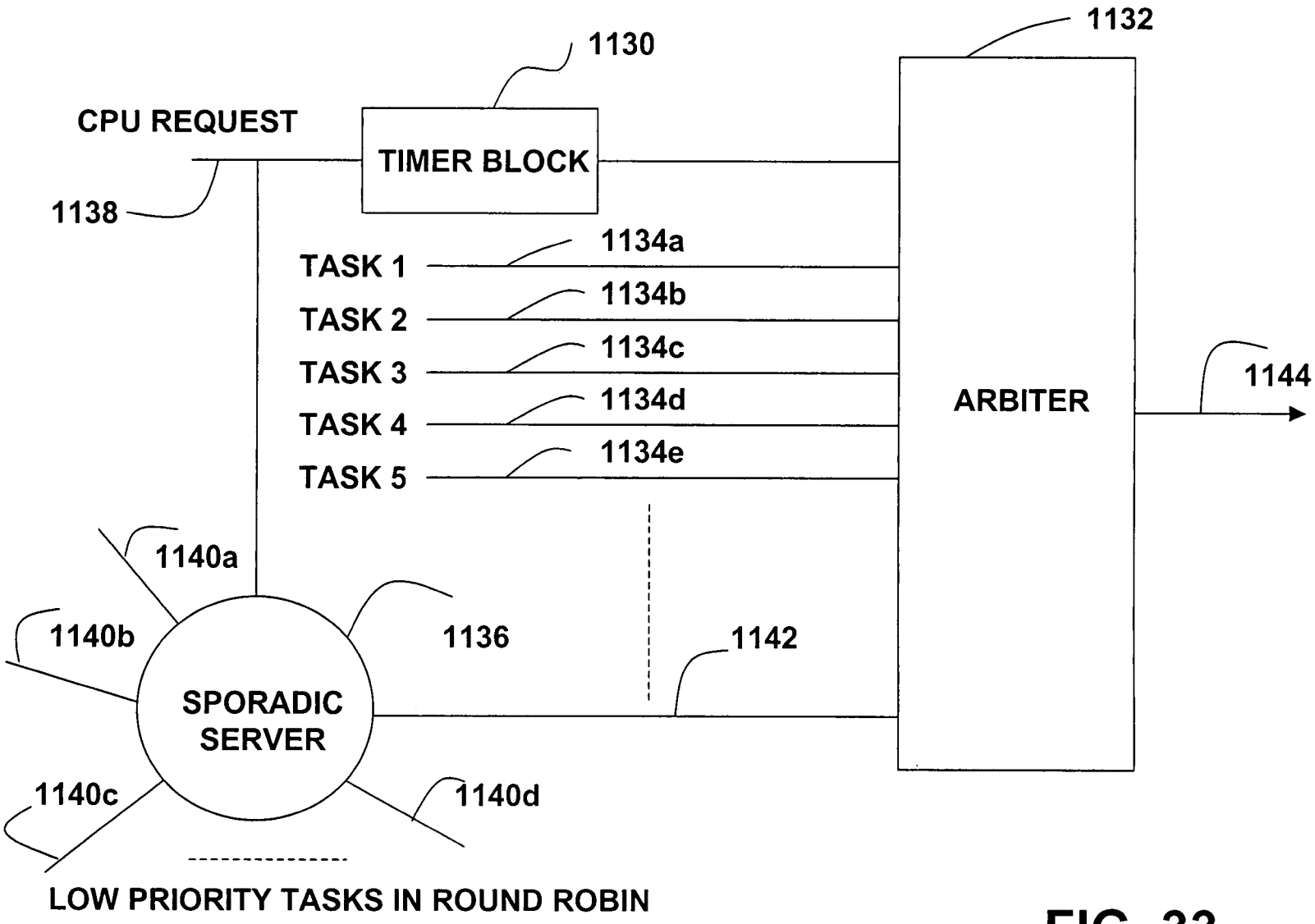

FIG. 33

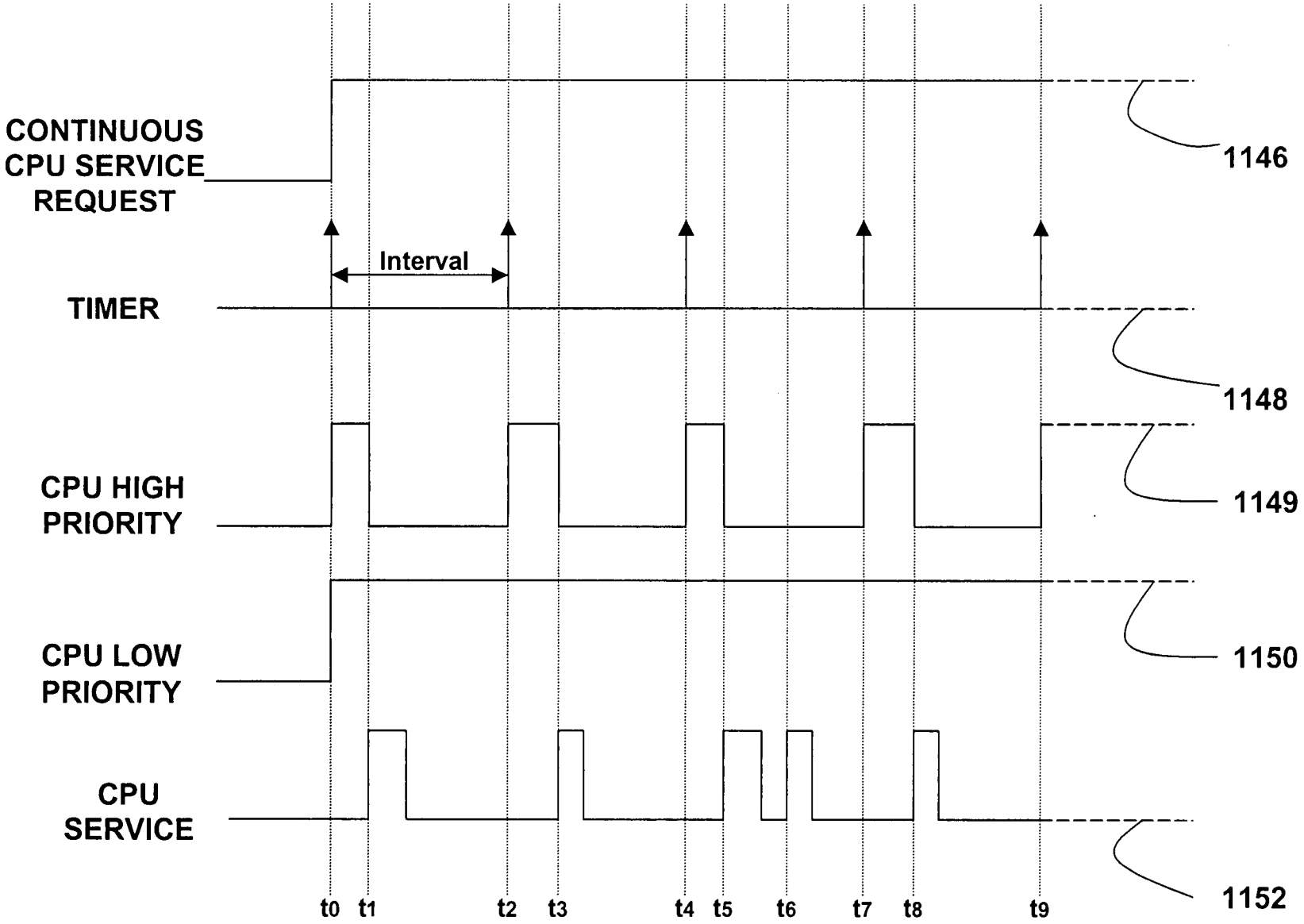

FIG. 34

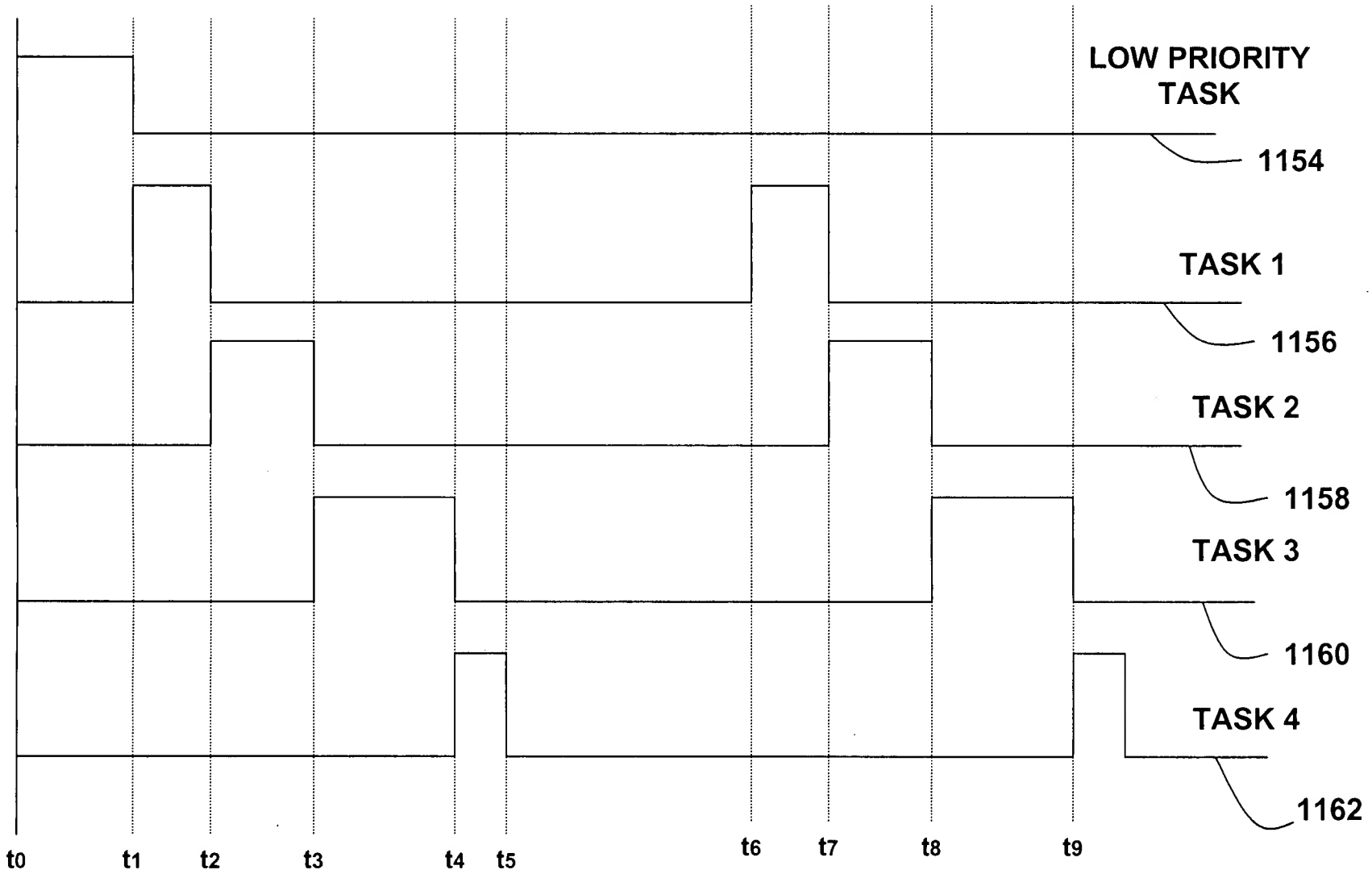

FIG. 35

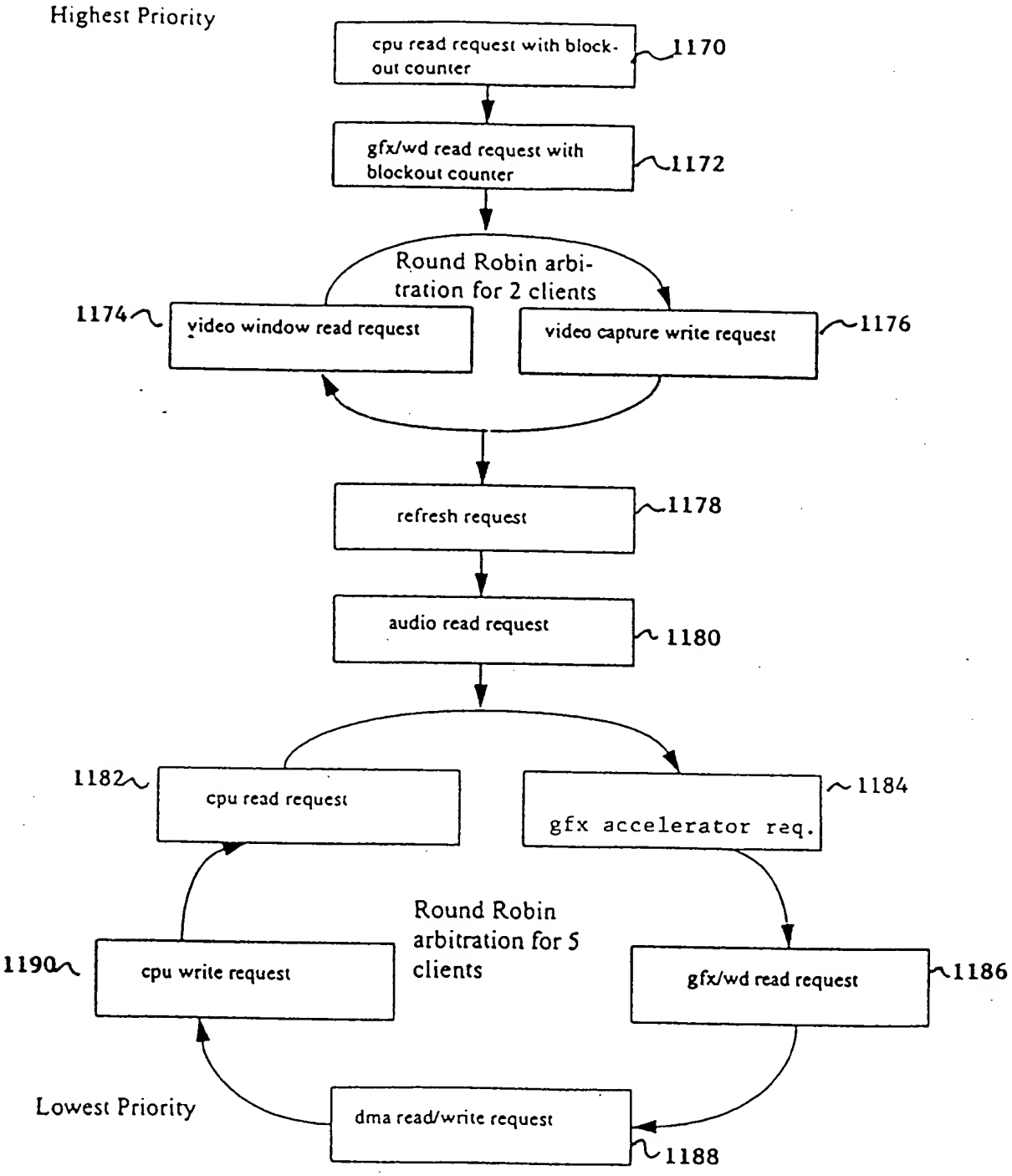
Highest Priority
cpu read request with block-out counter
1170
gfx/wd read request with blockout counter
1172
Round Robin arbitration for 2 clients
1174
video window read request
video capture write request
1176
refresh request
1178
audio read request
1180
1182
cpu read request
gfx accelerator req.
1184
Round Robin arbitration for 5 clients
1190
cpu write request
gfx/wd read request
1186
Lowest Priority
dma read/write request
1188

FIG. 36

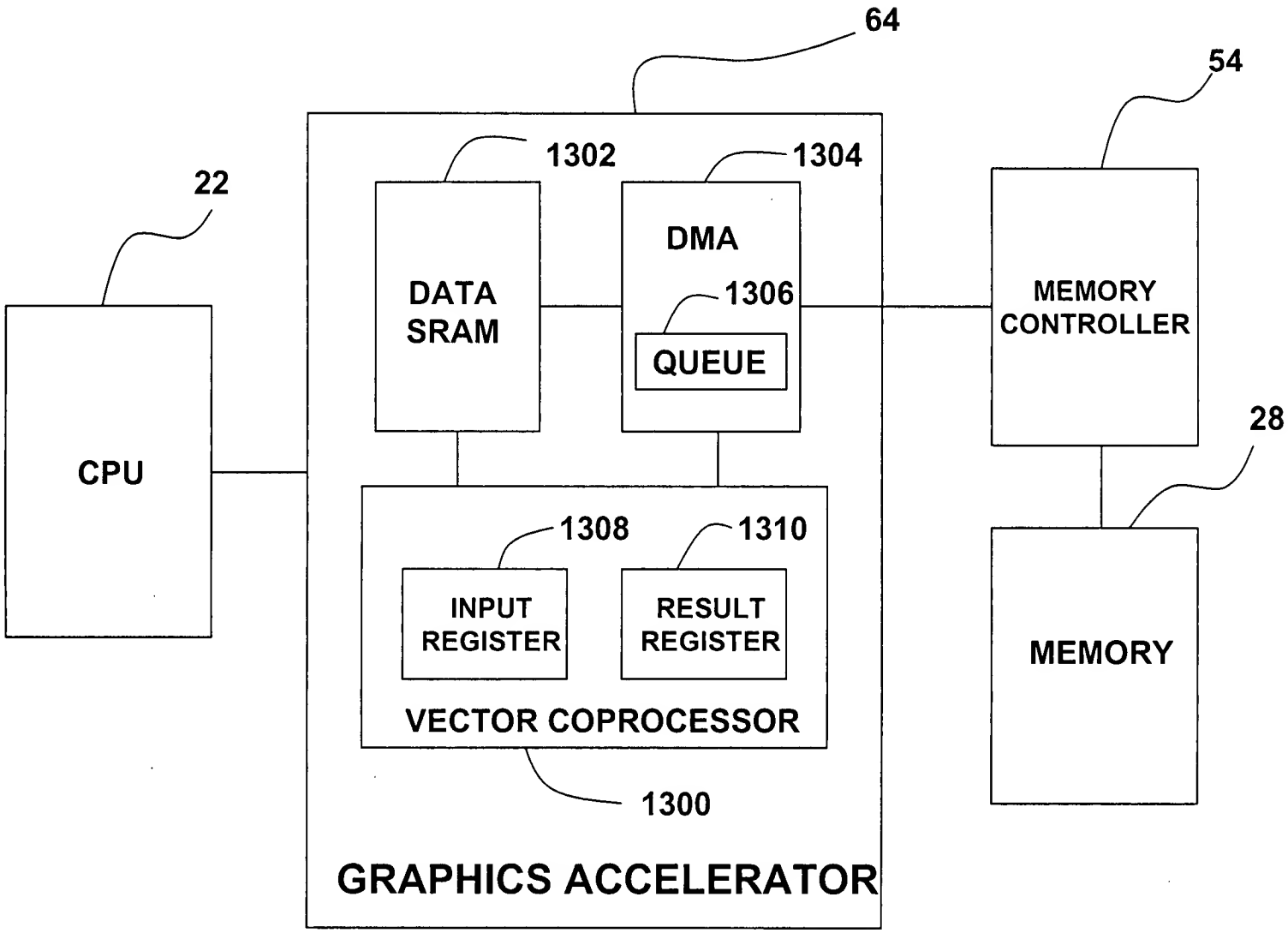

FIG. 37

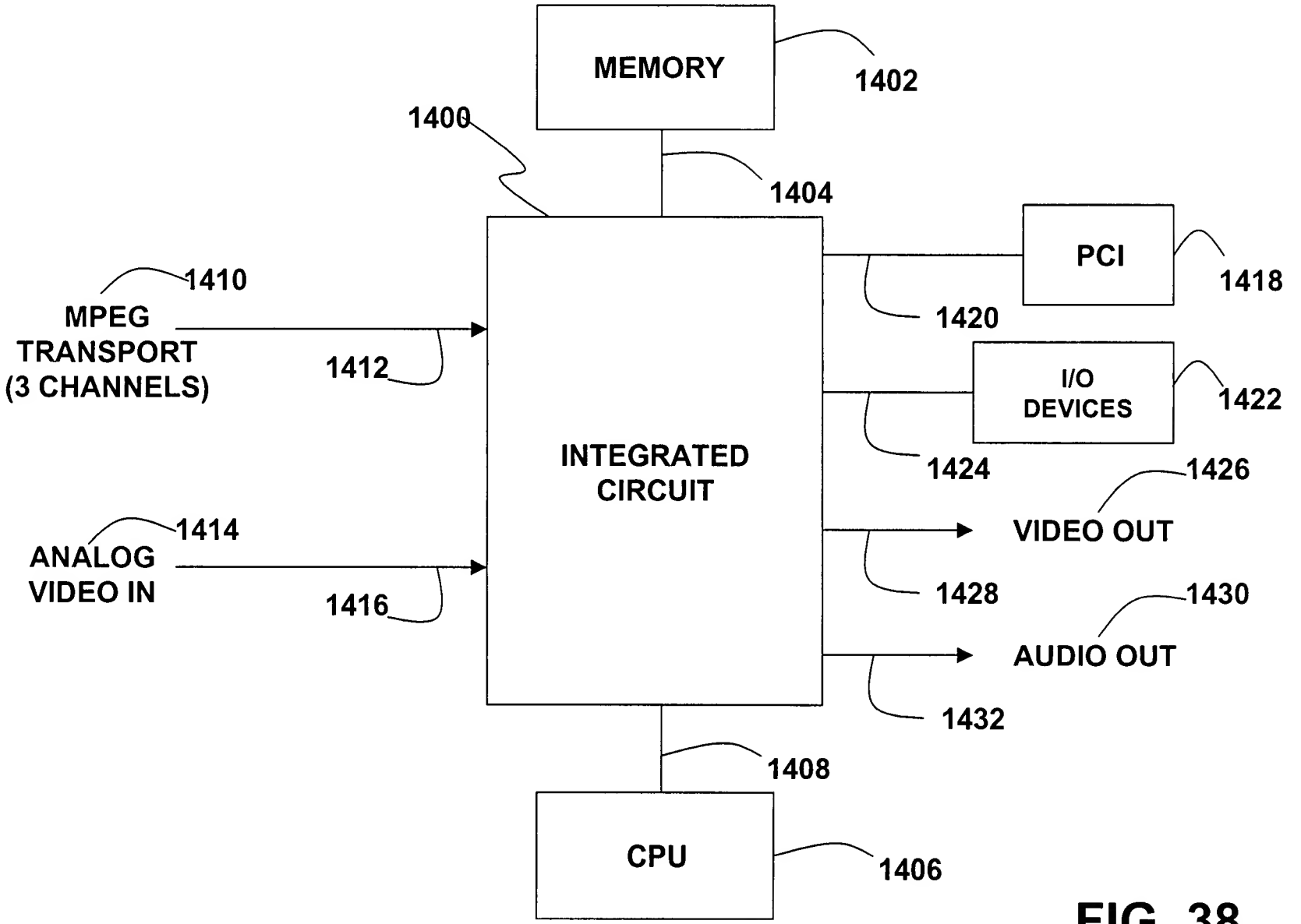

FIG. 38

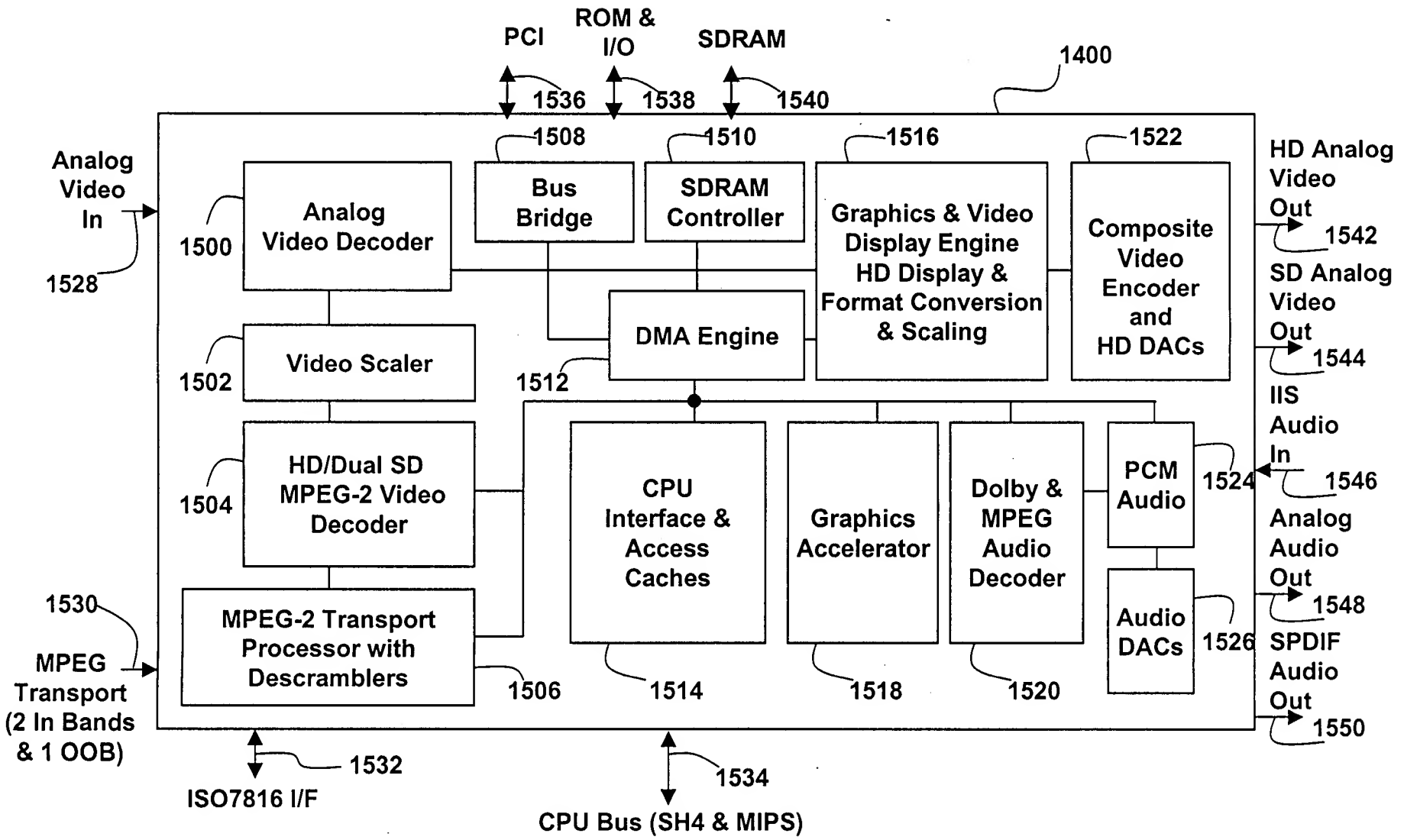
PCI
ROM & I/O
SDRAM
1400
1536
1538
1540
1508
1510
1516
1522
Analog Video In
1528
1500
Analog Video Decoder
Bus Bridge
SDRAM Controller
Graphics & Video Display Engine HD Display & Format Conversion & Scaling
Composite Video Encoder and HD DACs
HD Analog Video Out
1542
SD Analog Video Out
1544
1502
Video Scaler
1512
DMA Engine
IIS Audio In
1546
1504
HD/Dual SD MPEG-2 Video Decoder
CPU Interface & Access Caches
Graphics Accelerator
Dolby & MPEG Audio Decoder
PCM Audio
1524
Analog Audio Out
1548
1530
MPEG Transport (2 In Bands & 1 OOB)
MPEG-2 Transport Processor with Descramblers
1506
1514
1518
1520
Audio DACs
1526
SPDIF Audio Out
1550
1532
ISO7816 I/F
1534
CPU Bus (SH4 & MIPS)

FIG. 39

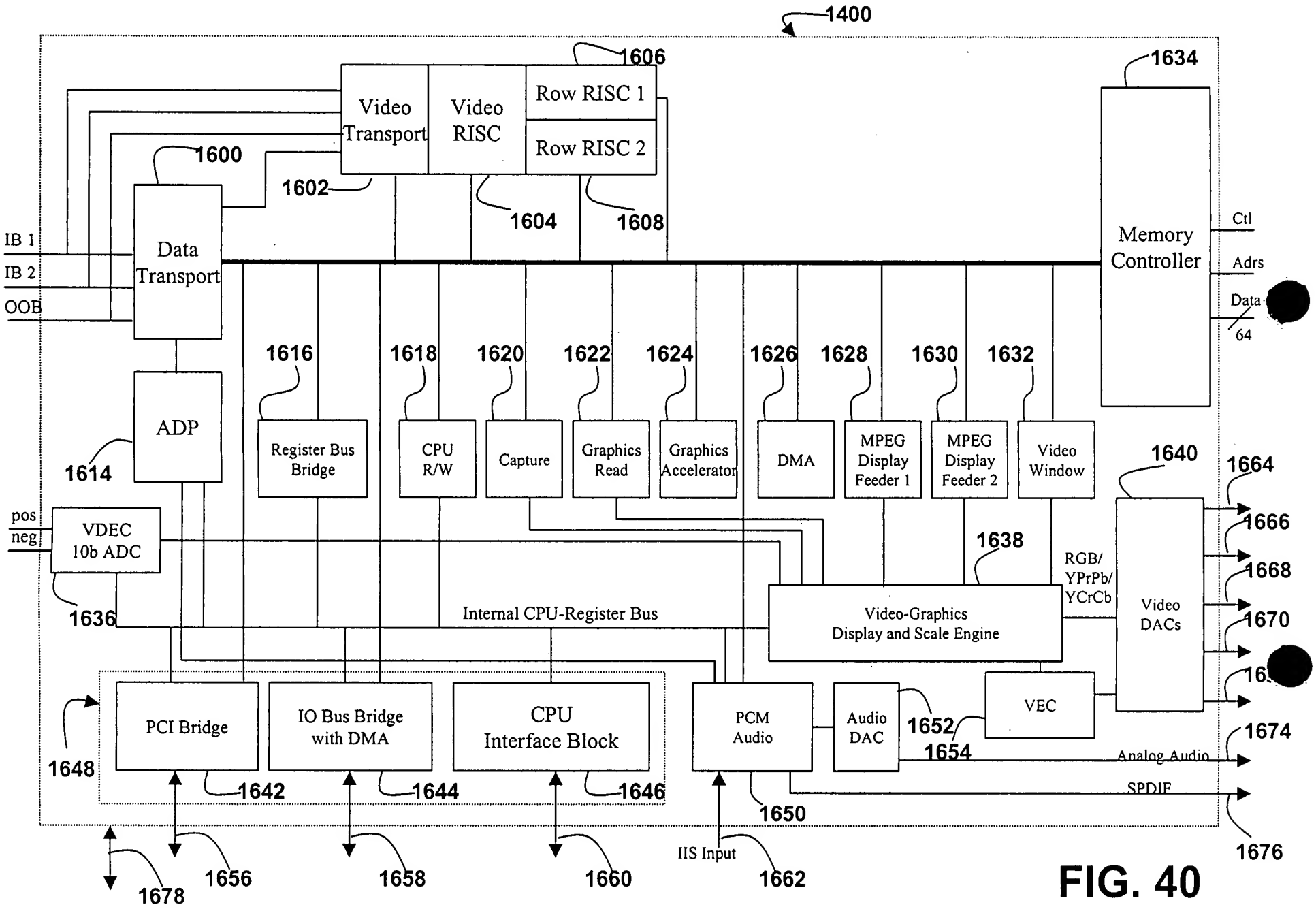

FIG. 40

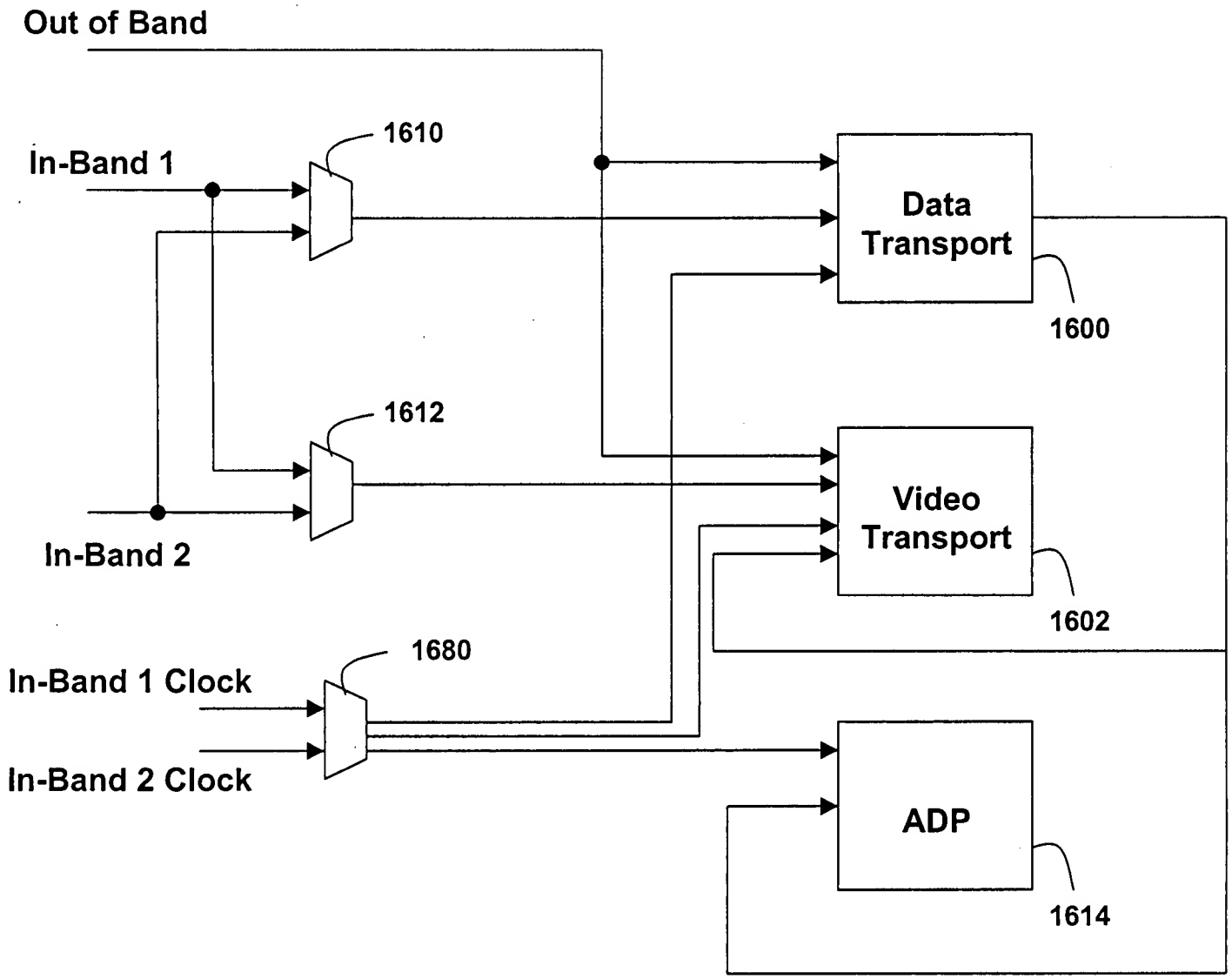
Out of Band
In-Band 1
1610
Data Transport
1600
1612
Video Transport
1602
In-Band 2
1680
In-Band 1 Clock
In-Band 2 Clock
ADP
1614

FIG. 41

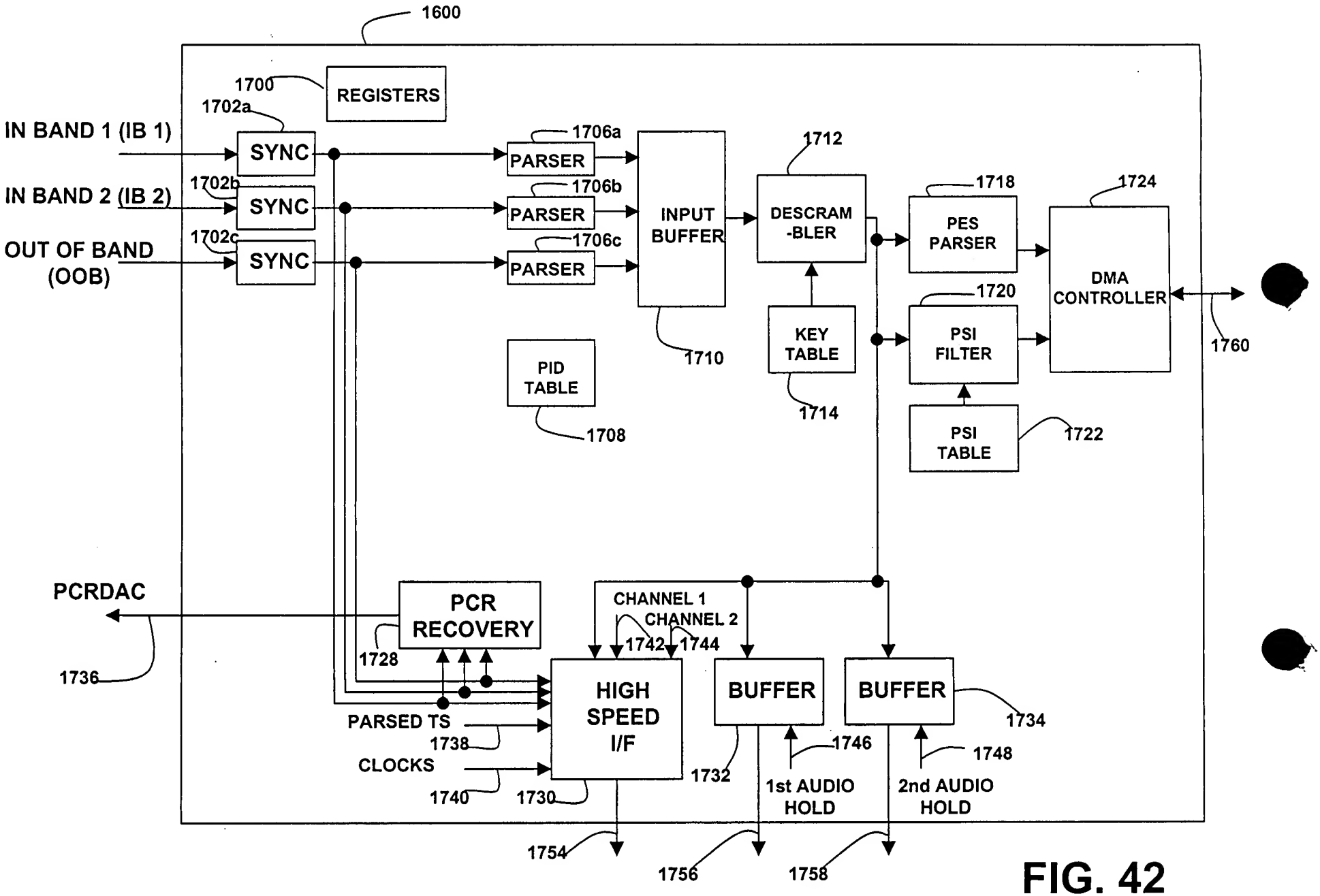

FIG. 42

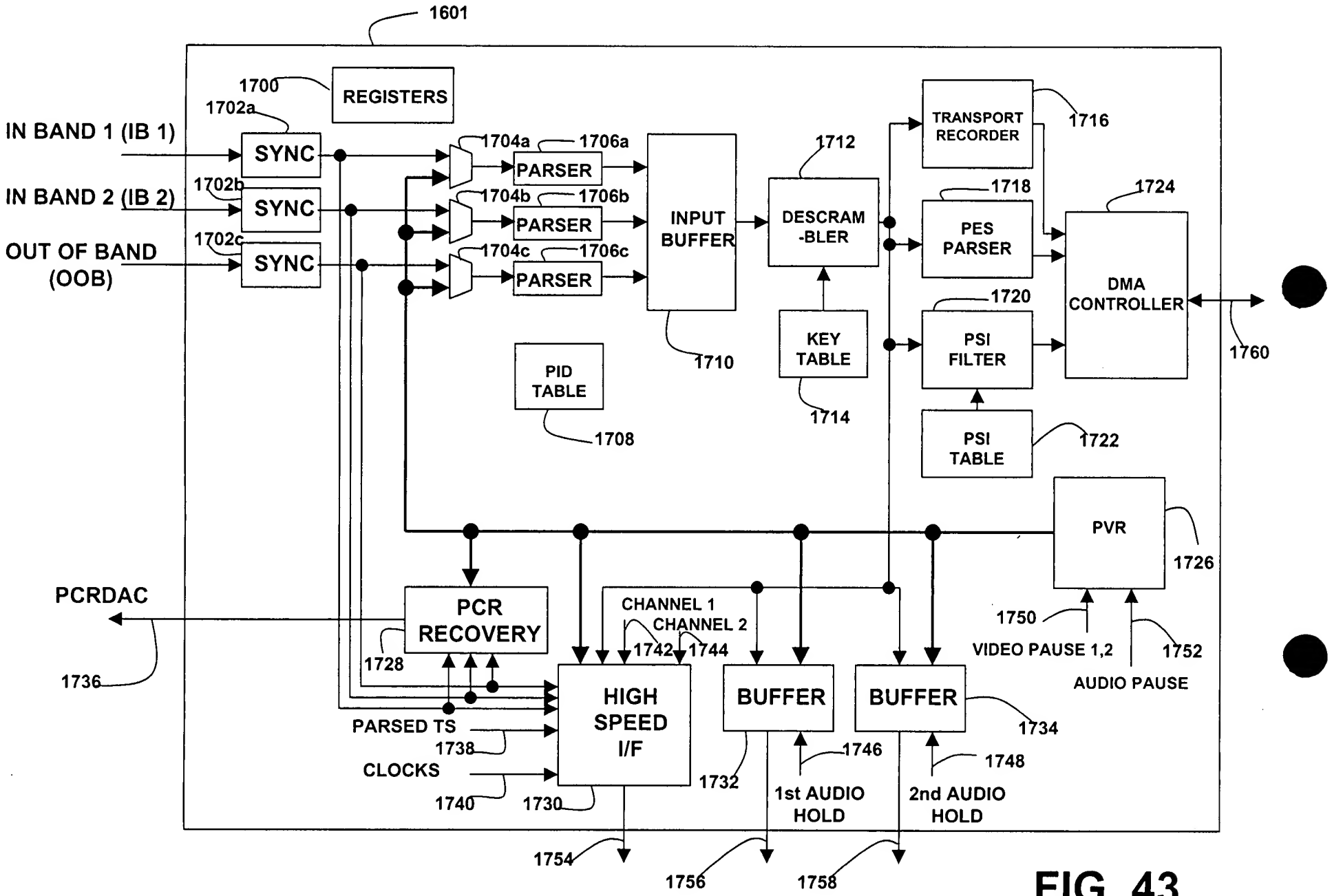

FIG. 43

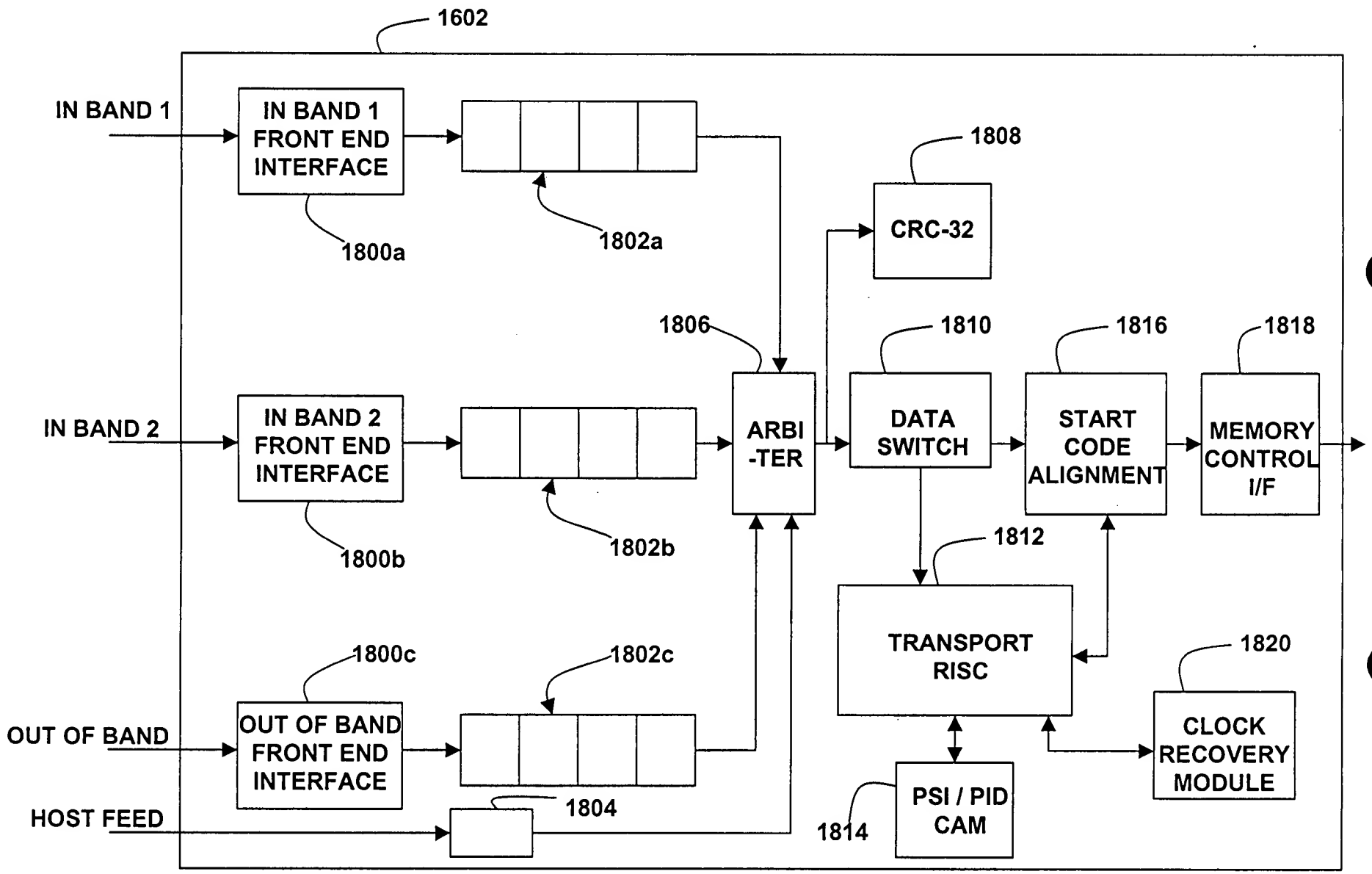
1602
IN BAND 1
IN BAND 1 FRONT END INTERFACE
1800a
1802a
1808
CRC-32
1806
1810
1816
1818
IN BAND 2
IN BAND 2 FRONT END INTERFACE
1800b
1802b
ARBI -TER
DATA SWITCH
START CODE ALIGNMENT
MEMORY CONTROL I/F
1812
TRANSPORT RISC
1820
CLOCK RECOVERY MODULE
1800c
1802c
OUT OF BAND
OUT OF BAND FRONT END INTERFACE
1804
HOST FEED
1814
PSI / PID CAM

FIG. 44

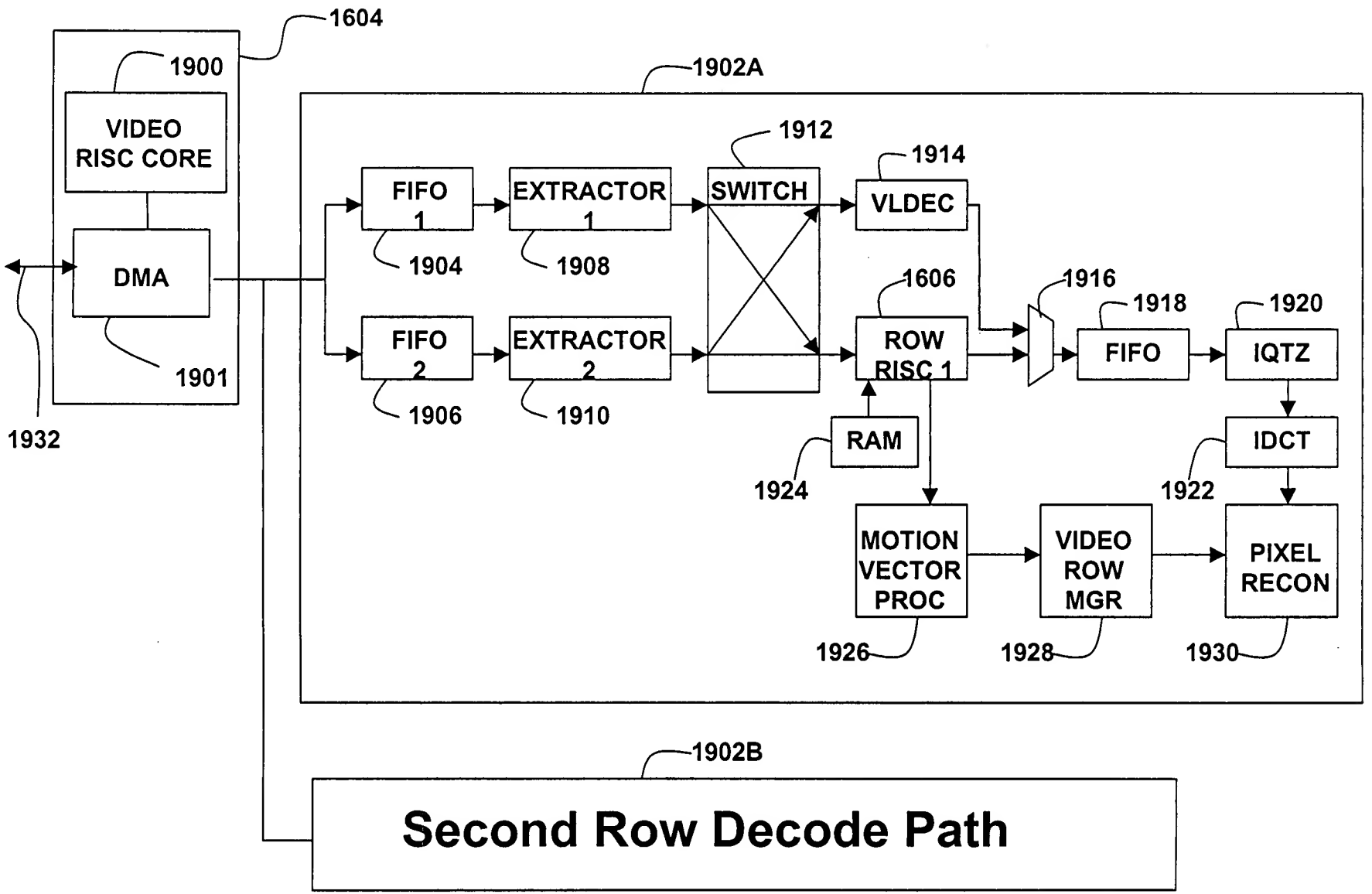

FIG. 45

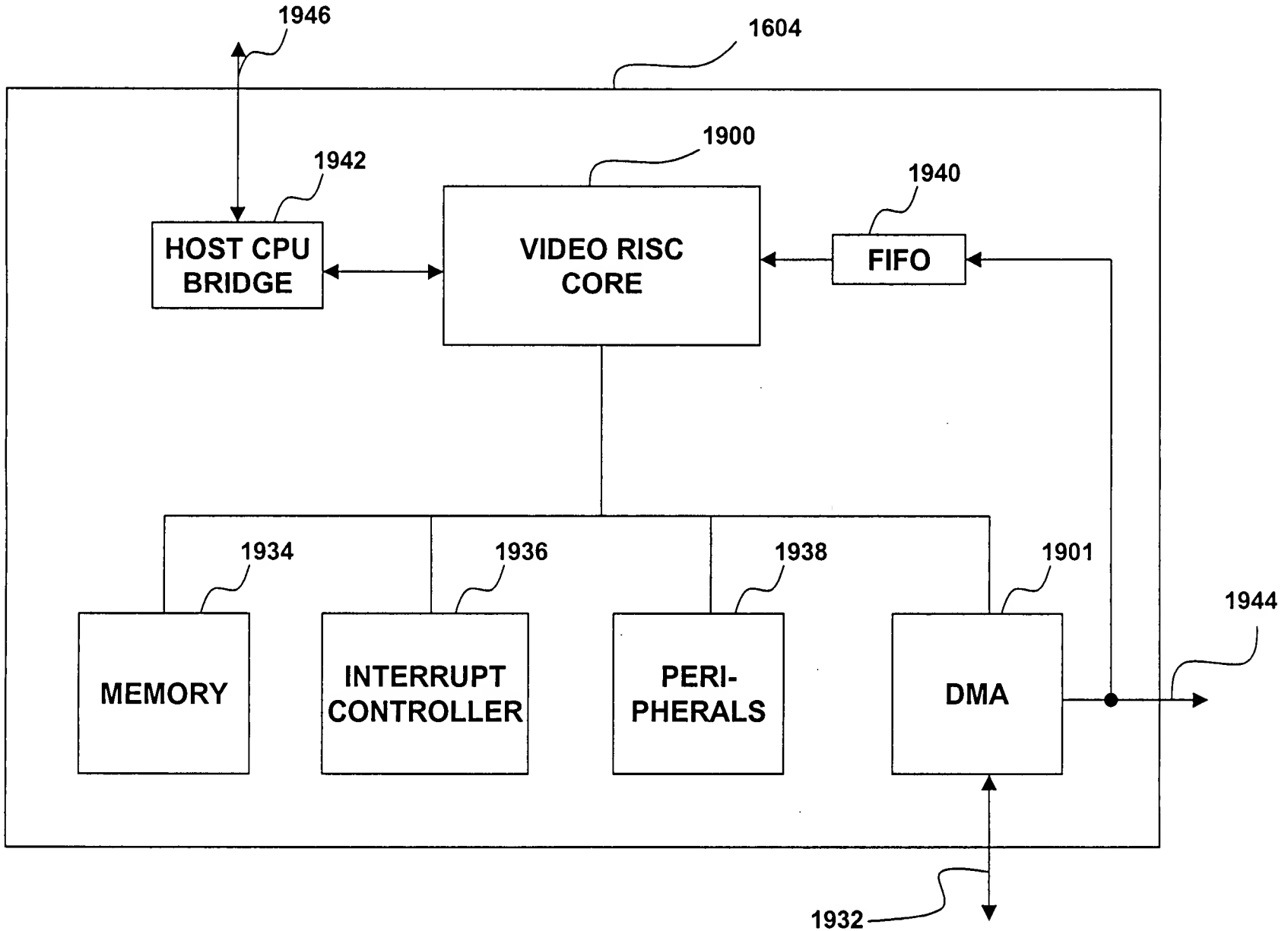

FIG. 46

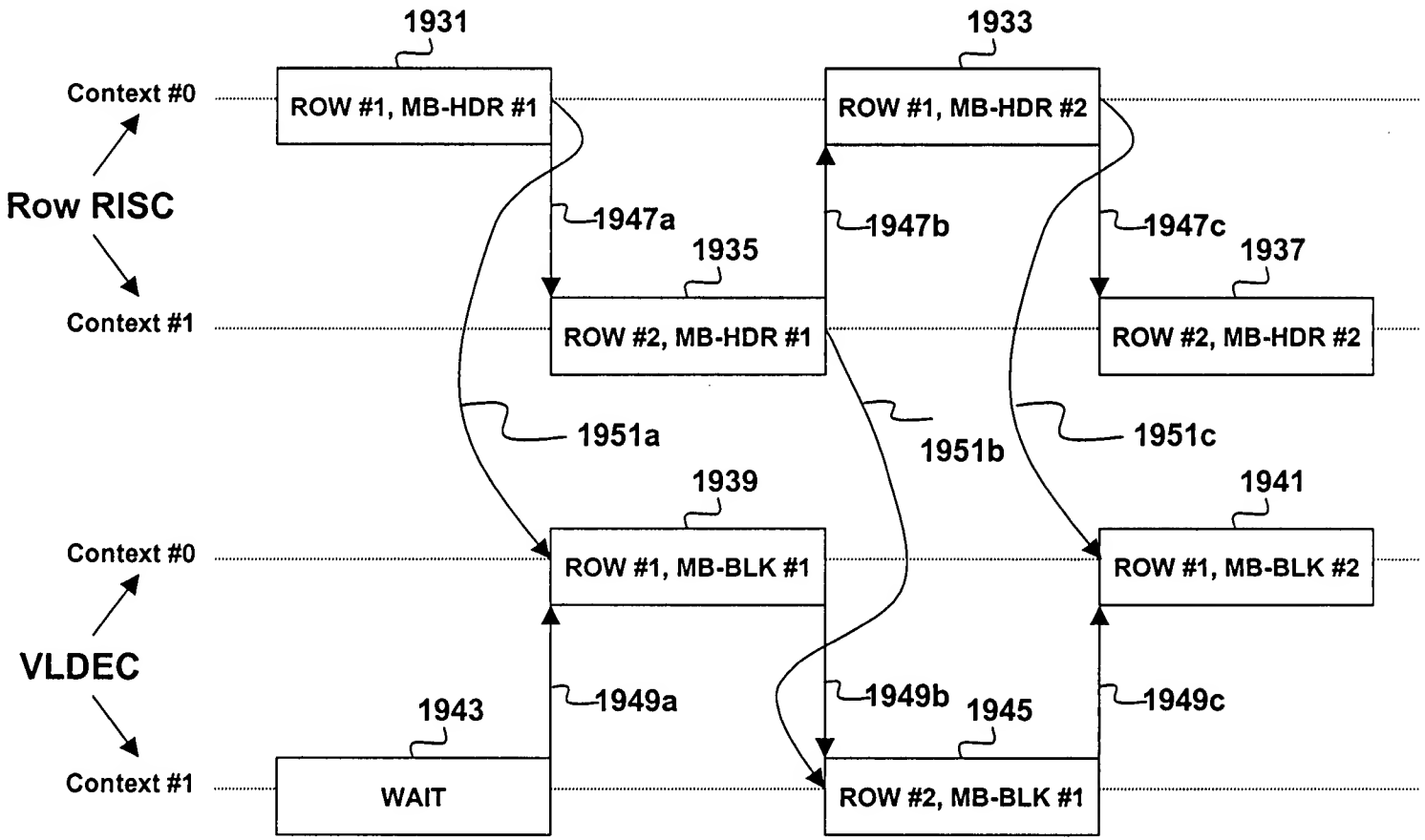

FIG. 47

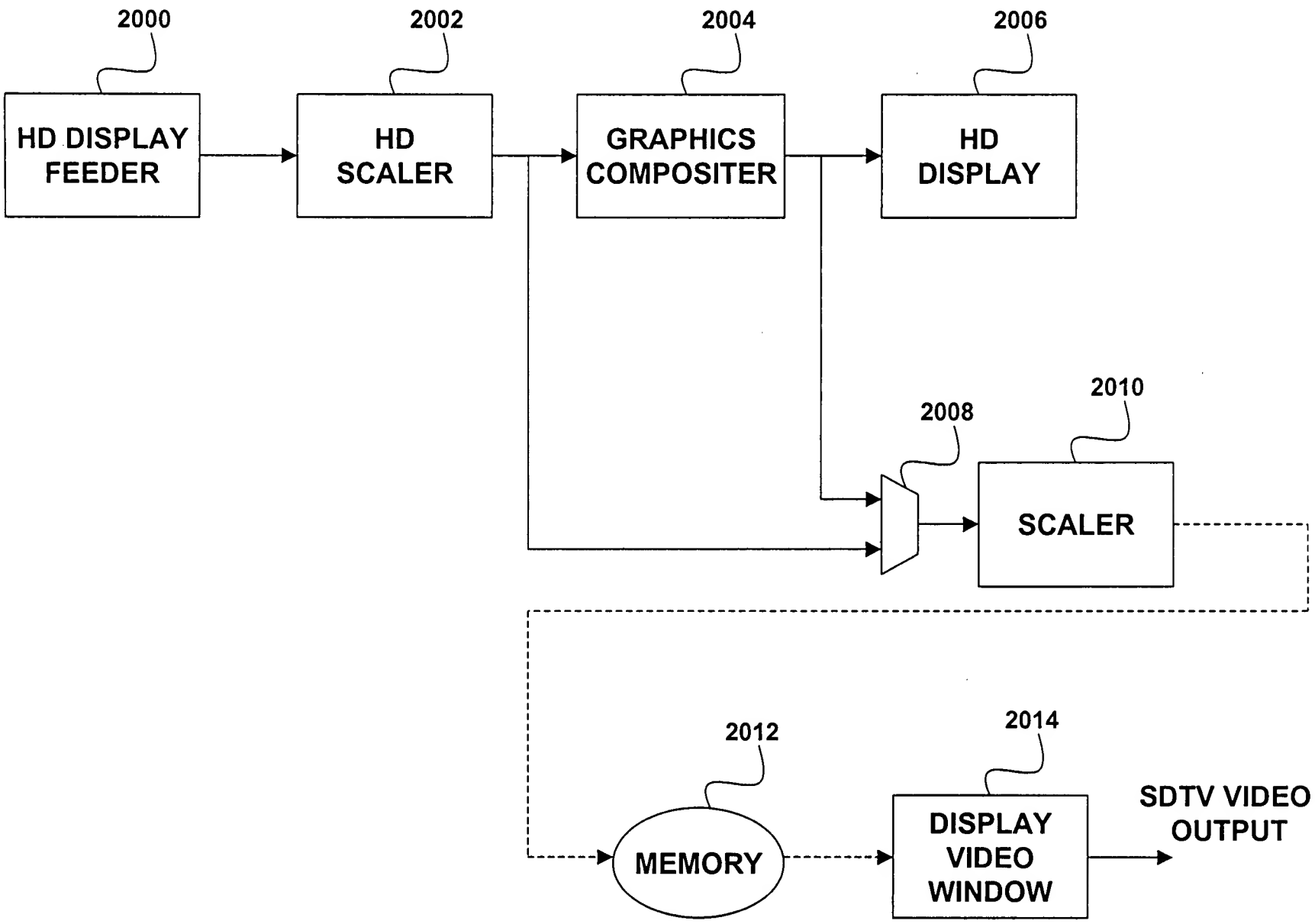

FIG. 48

MPEG VIDEO DECODING STAGES

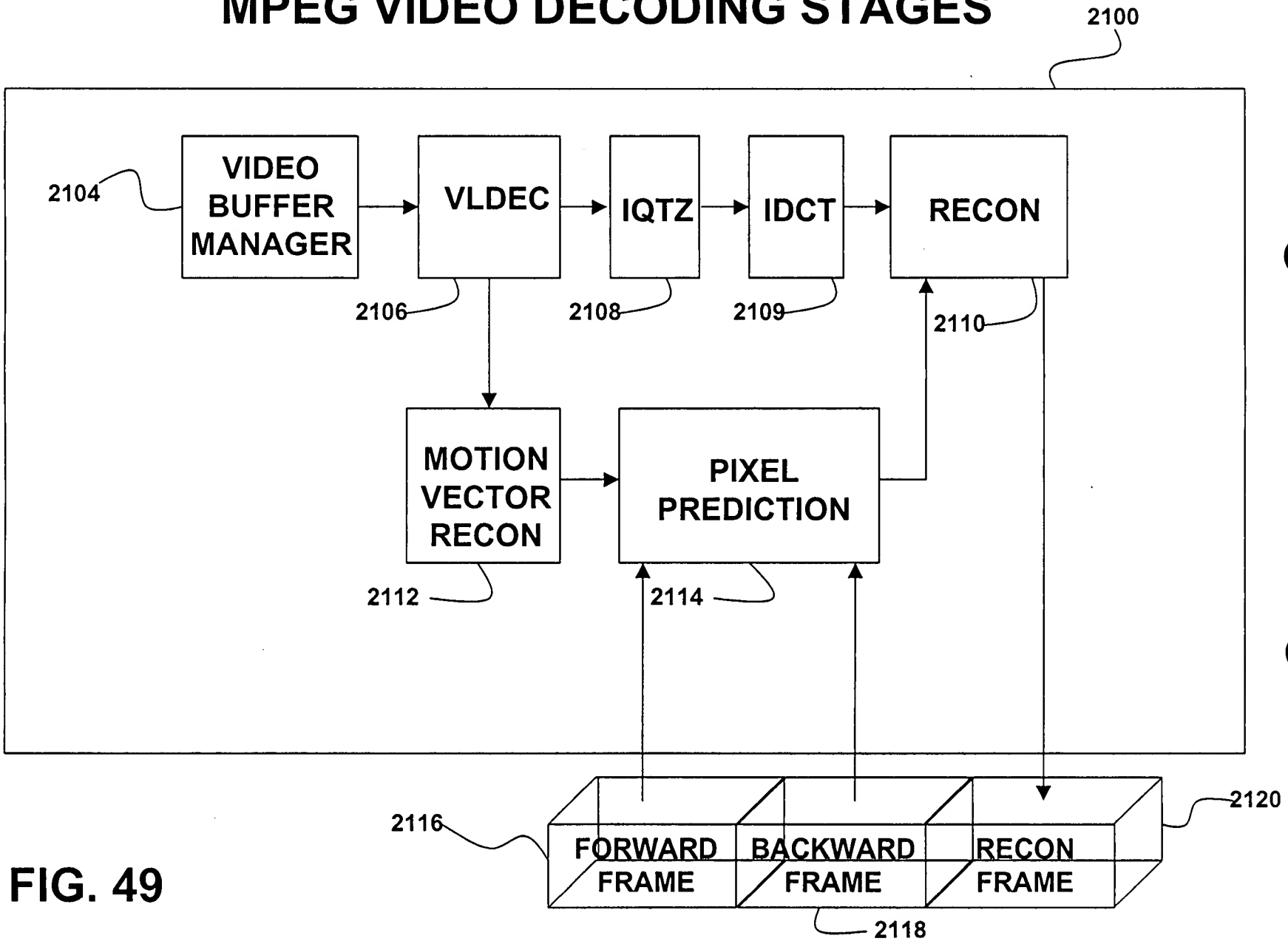

FIG. 49

MPEG VIDEO DECODING STAGES WITH VIDEO TIME DOWNSCALING

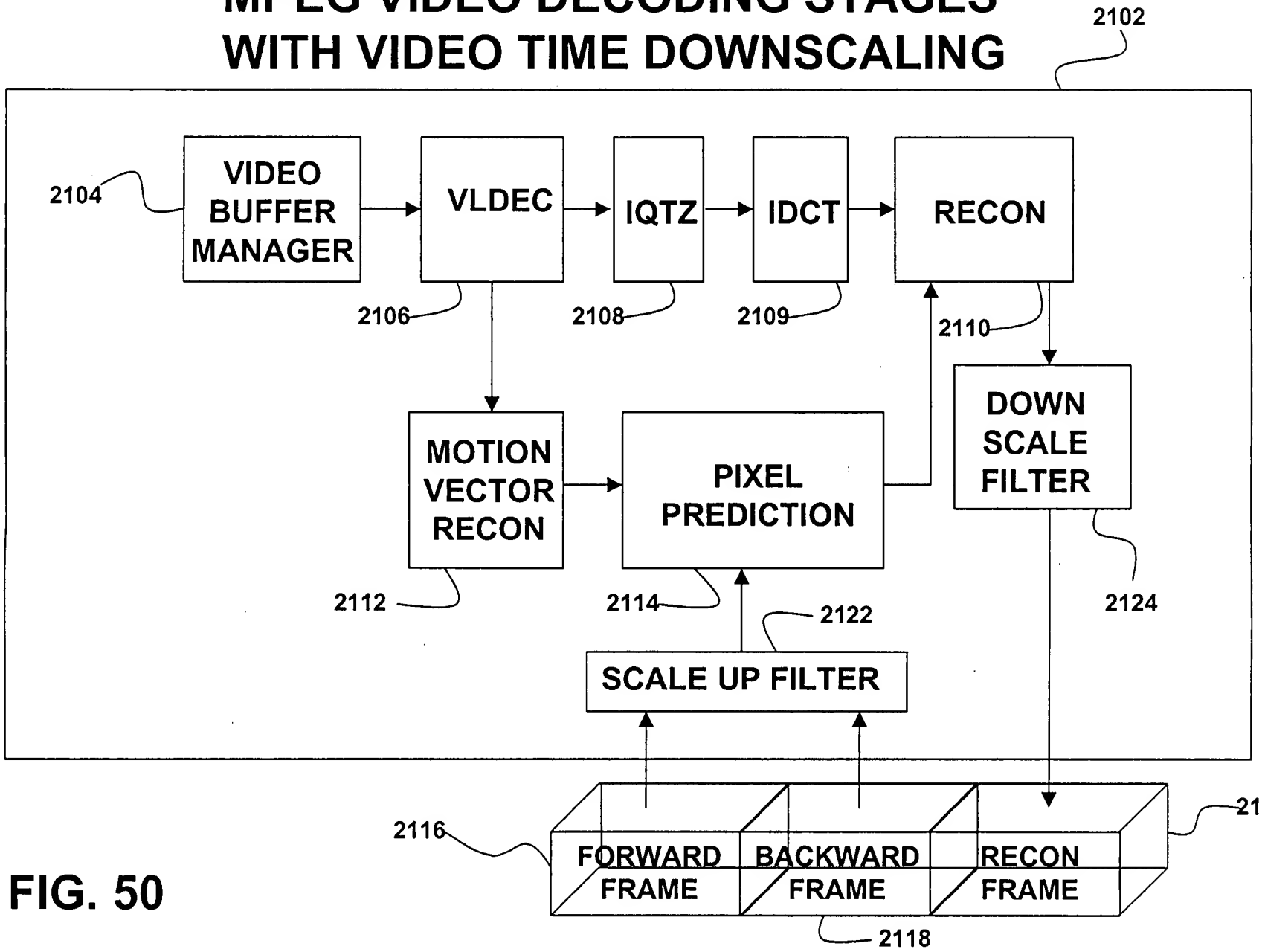

FIG. 50

FRAME-PREDICTION FOR I-PICTURES AND P-PICTURES

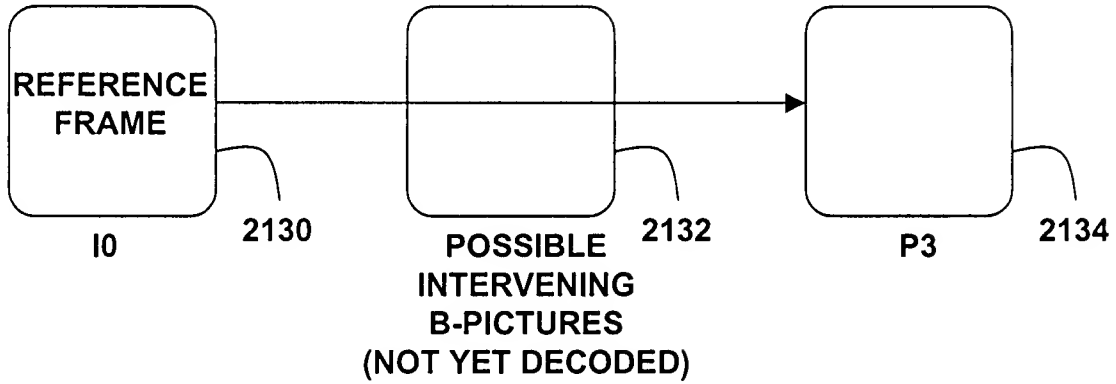

FIG. 51

FIELD PREDICTION IN A FRAME-PICTURE

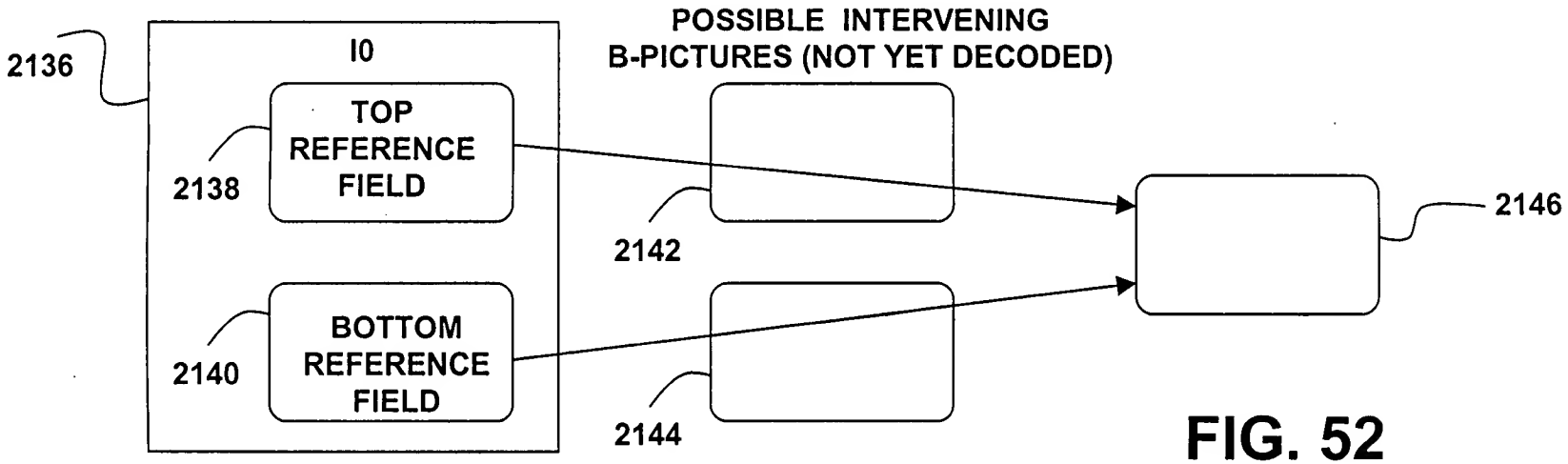

FIG. 52

PREDICTION OF THE FIRST FIELD-PICTURE

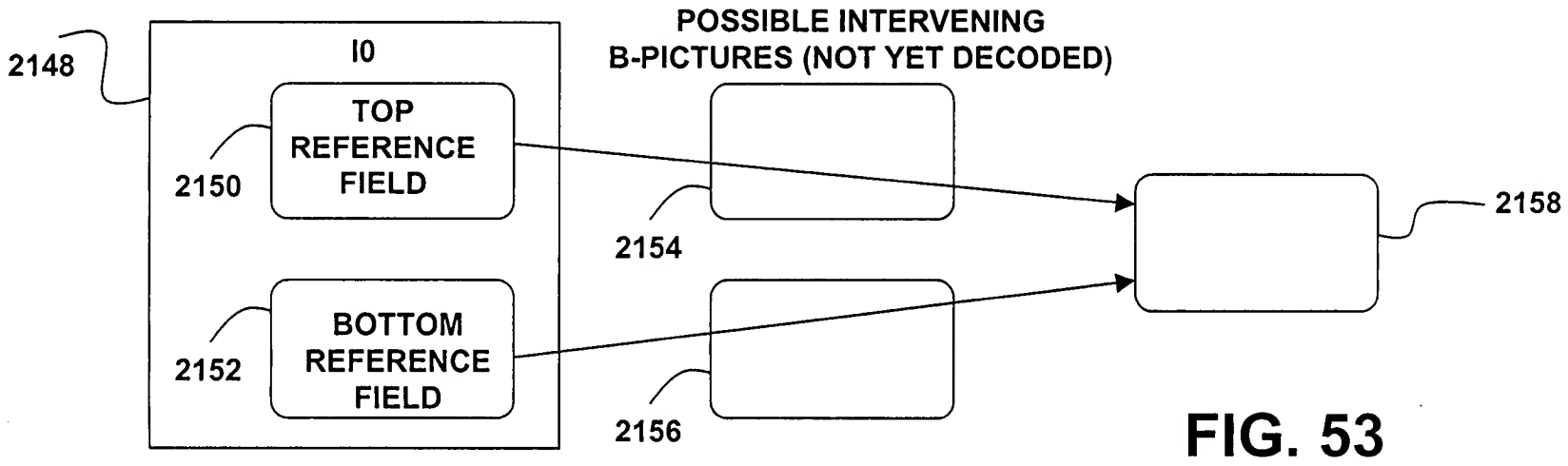

FIG. 53

PREDICTION OF THE "BOTTOM FIELD" SECOND FIELD-PICTURE

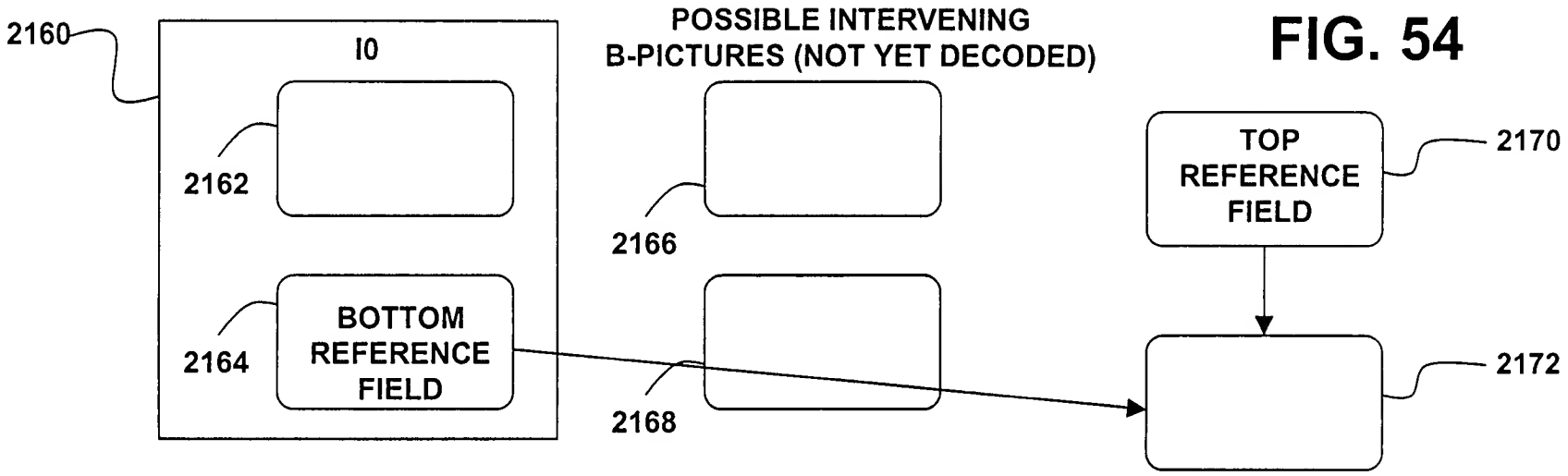

FIG. 54

PREDICTION OF THE "TOP FIELD" SECOND FIELD-PICTURE

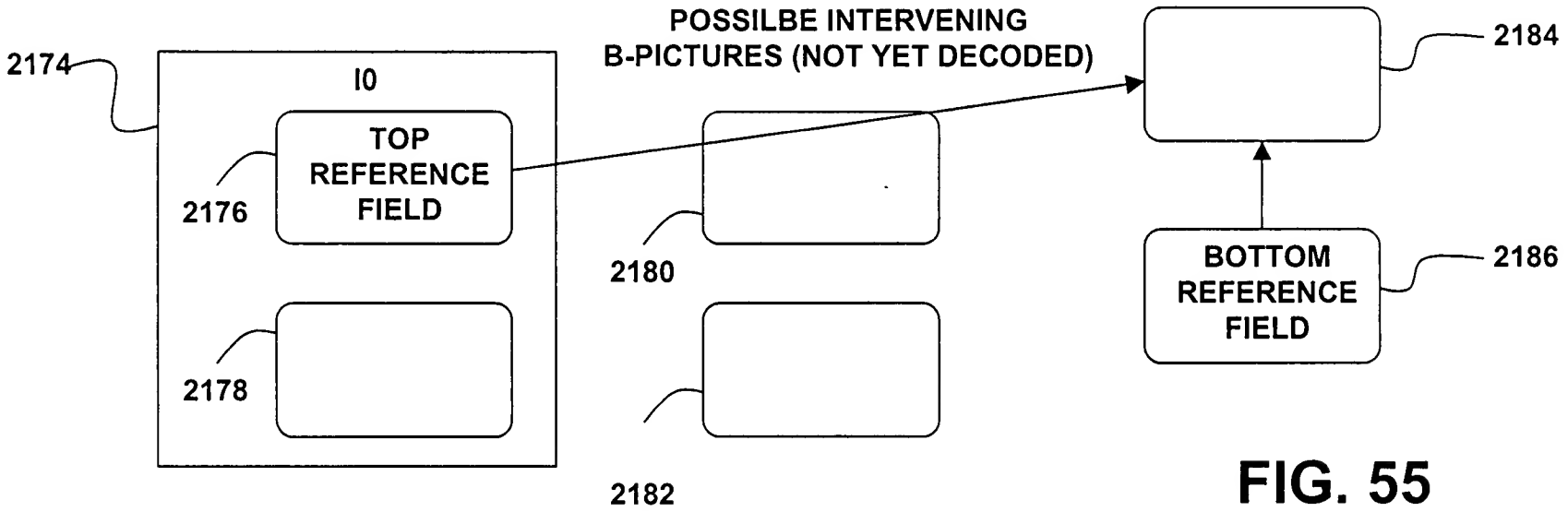

FIG. 55

FIELD-PREDICTIONOF B FIELD PICTURES OR B FRAME PICTURES

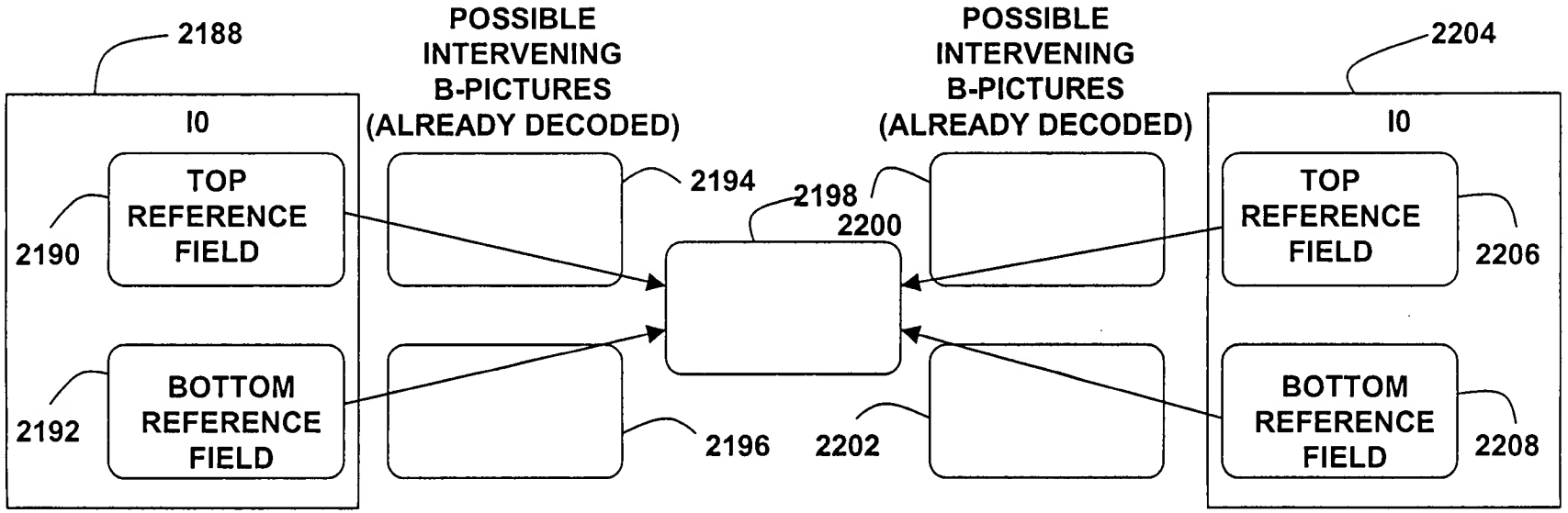

FIG. 56

FRAME-PREDICTIONS FOR B-PICTURES

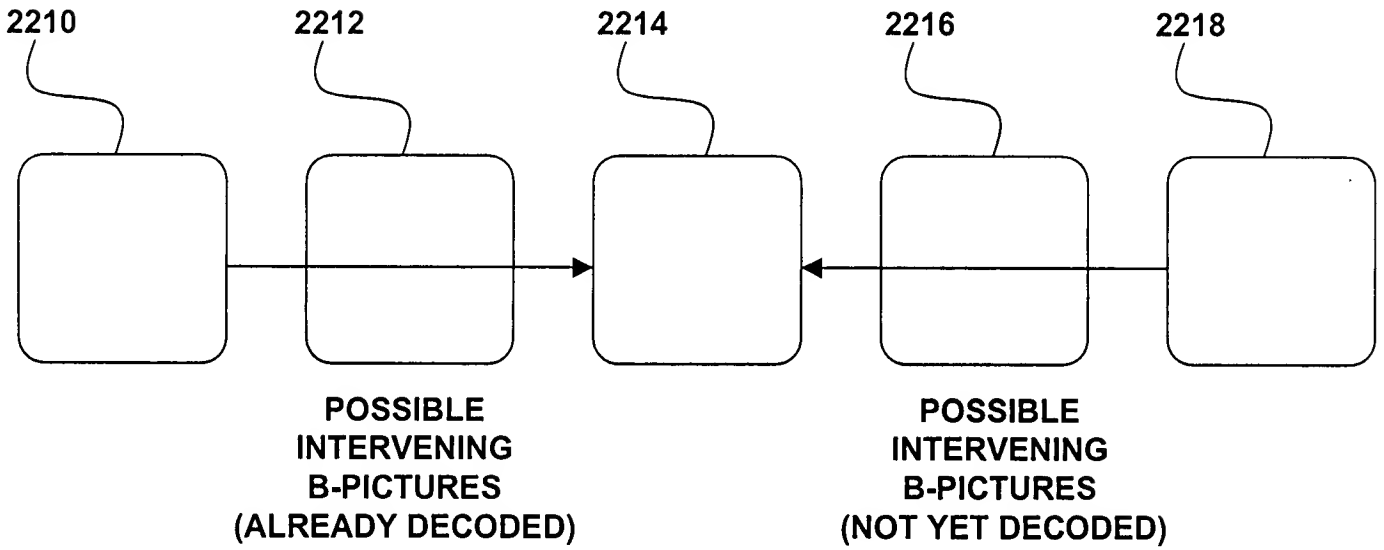

FIG. 57

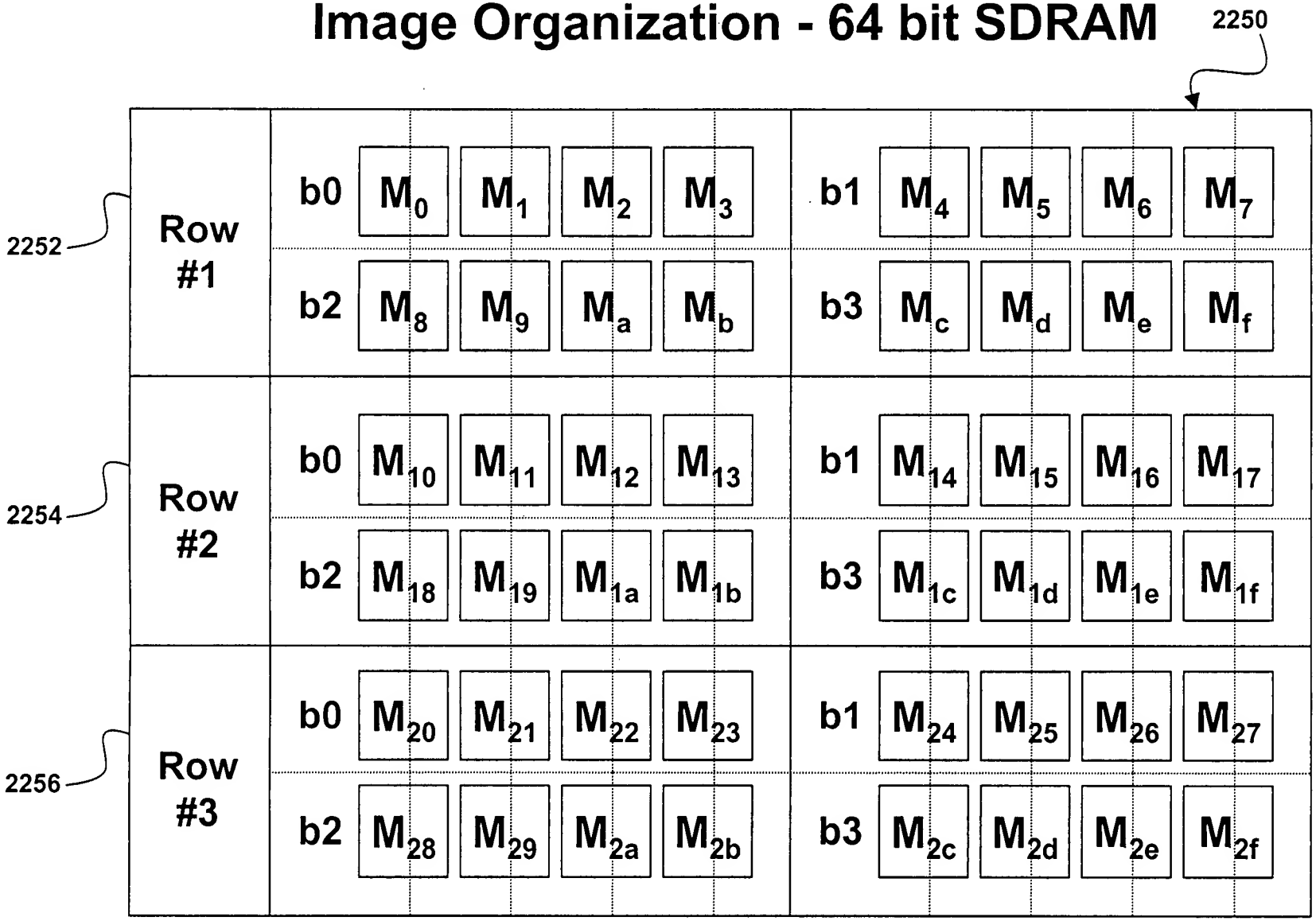

FIG. 58

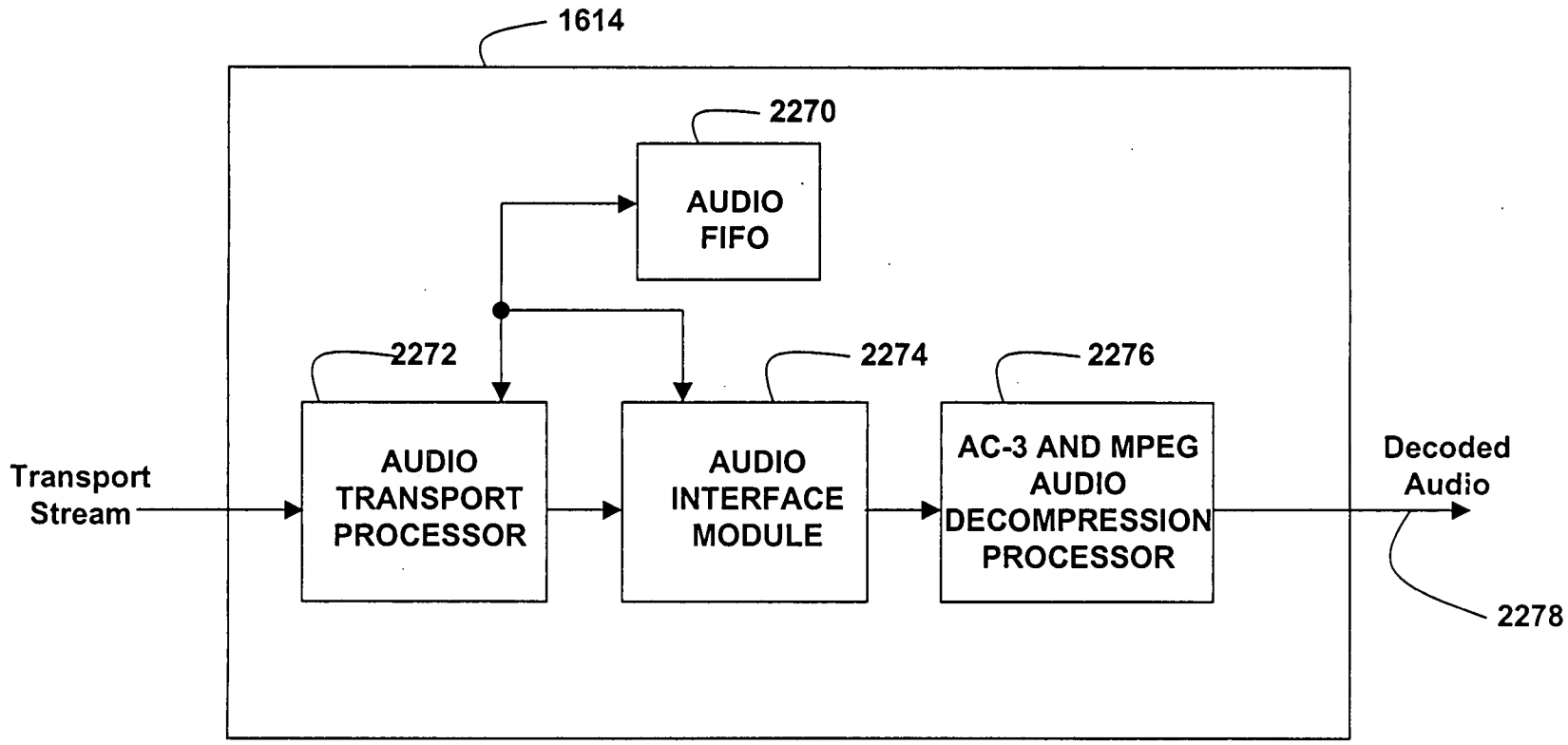

FIG. 59

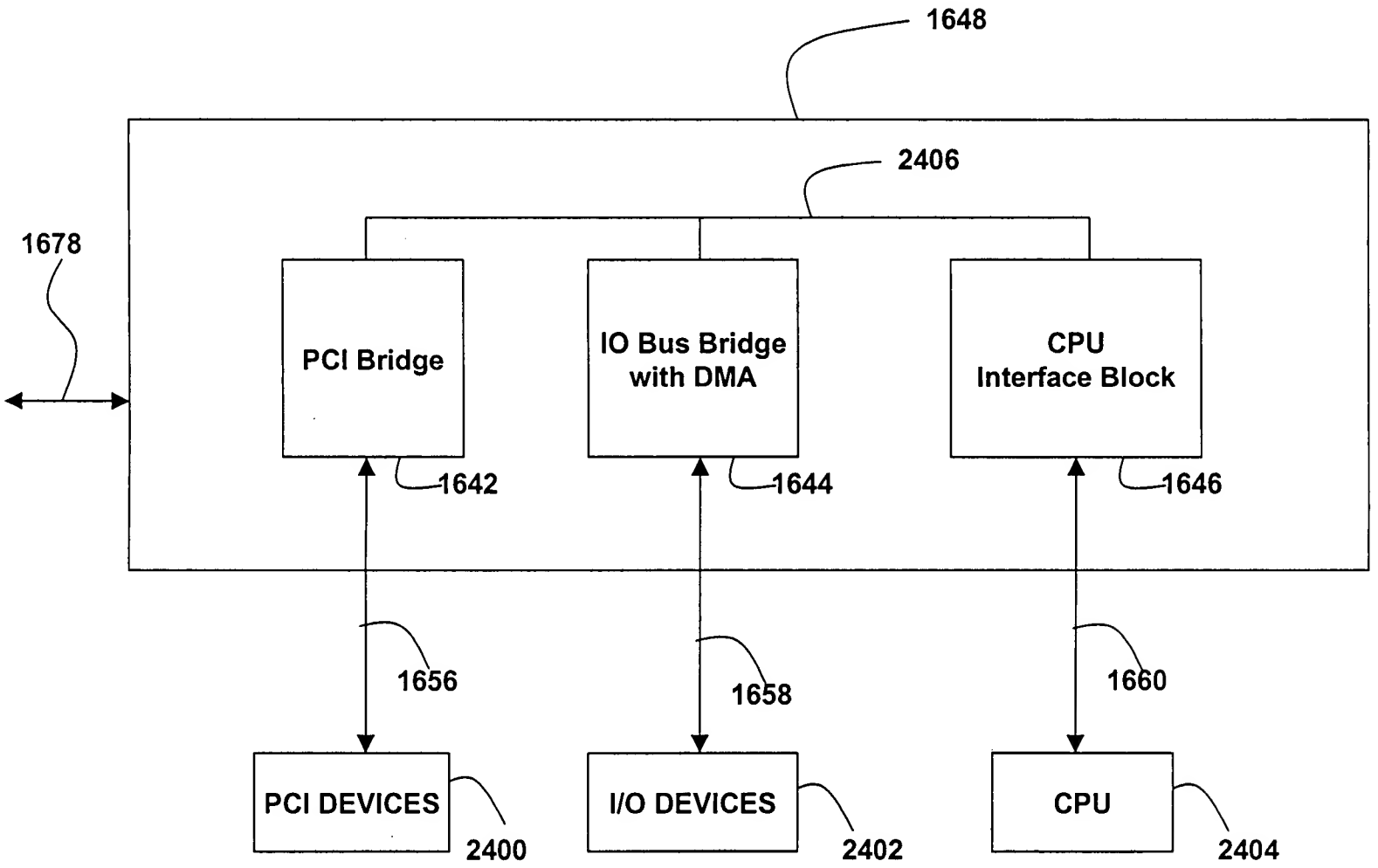

FIG. 60

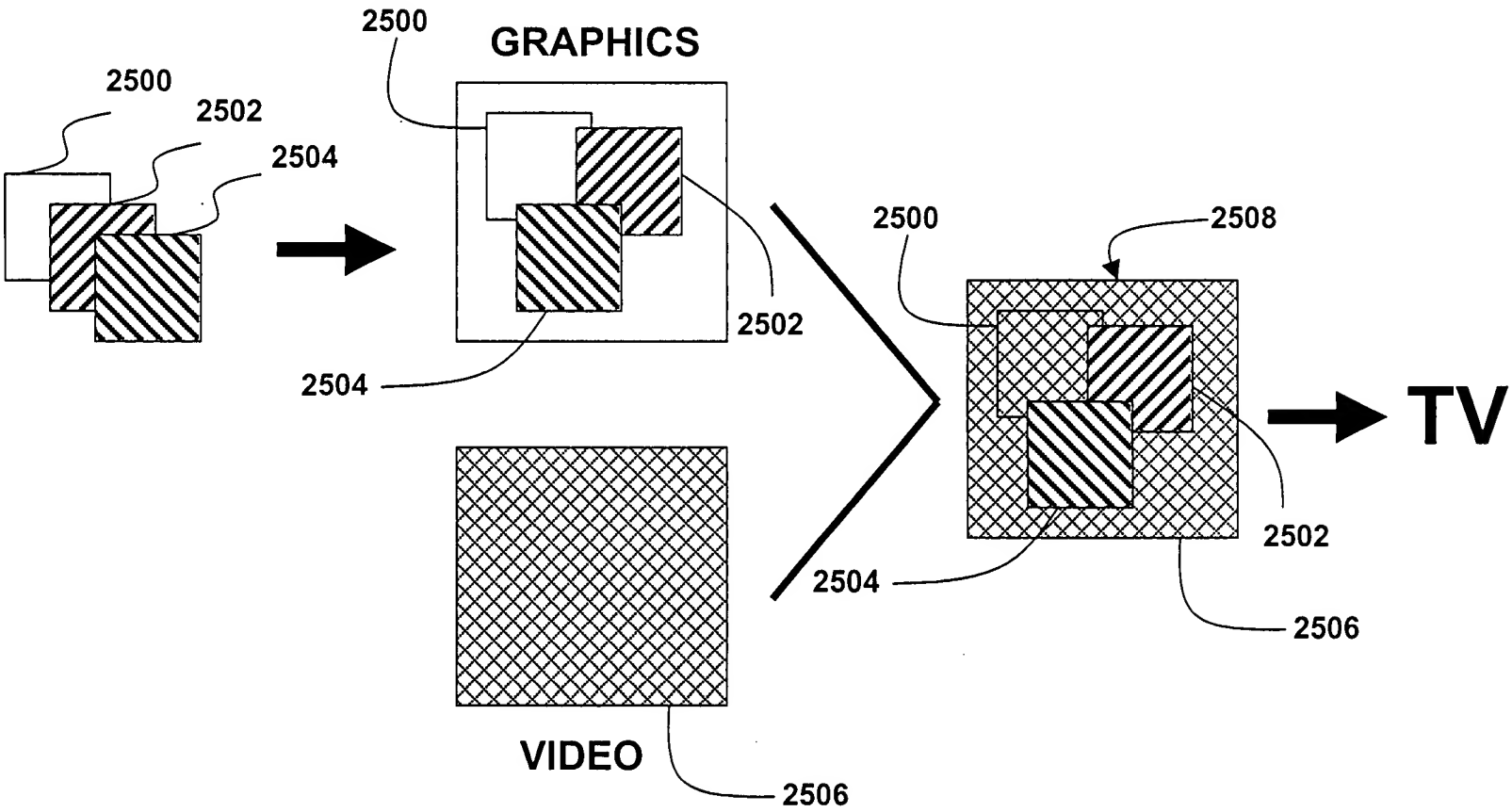
2500
2502
2504
2500
GRAPHICS
2502
2504
VIDEO
2506
2500
2508
2502
2504
2506
TV

FIG. 61

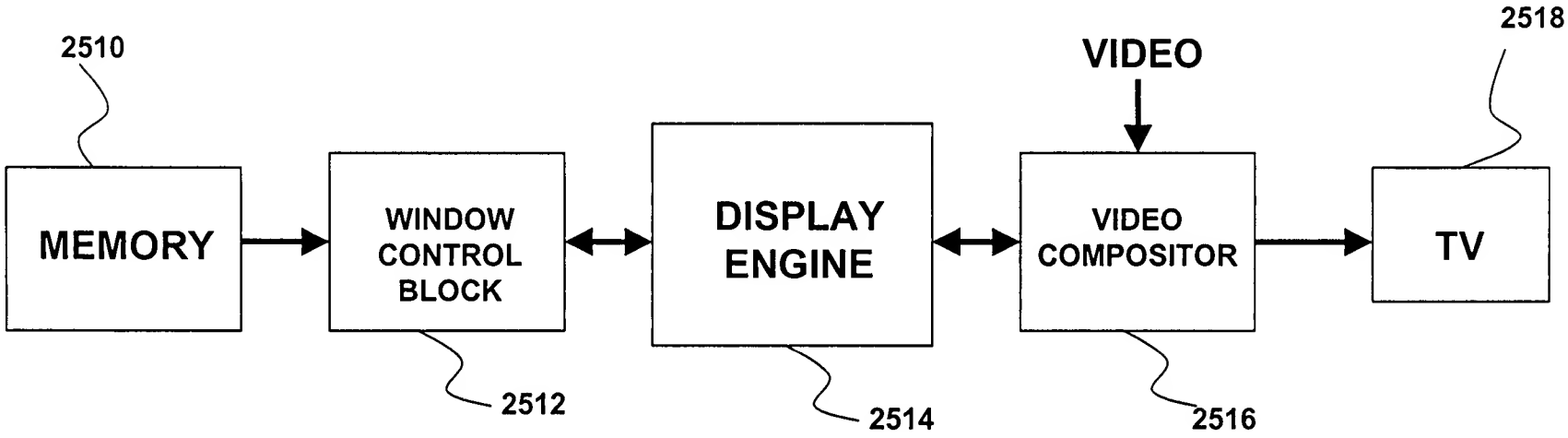

FIG. 62

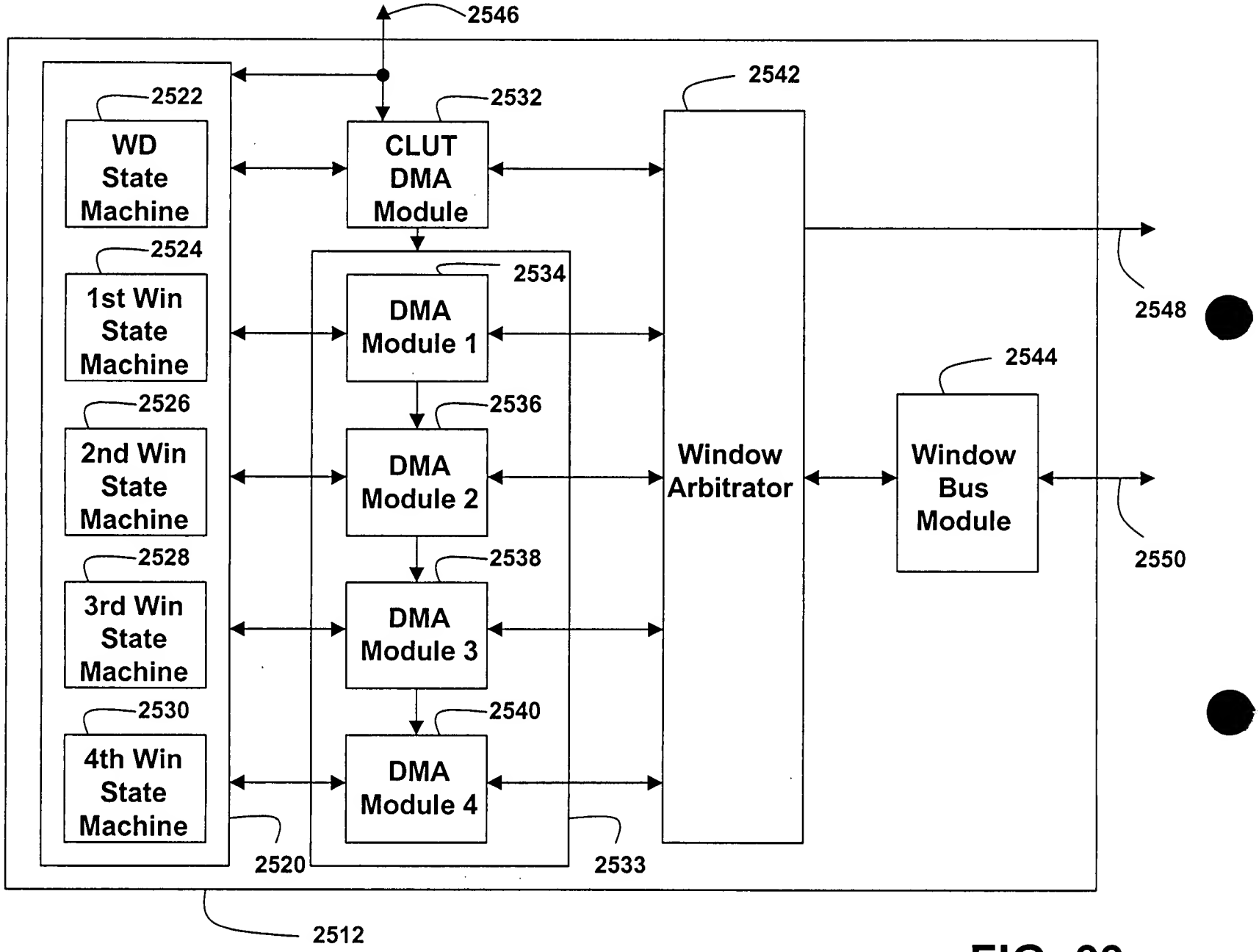

FIG. 63

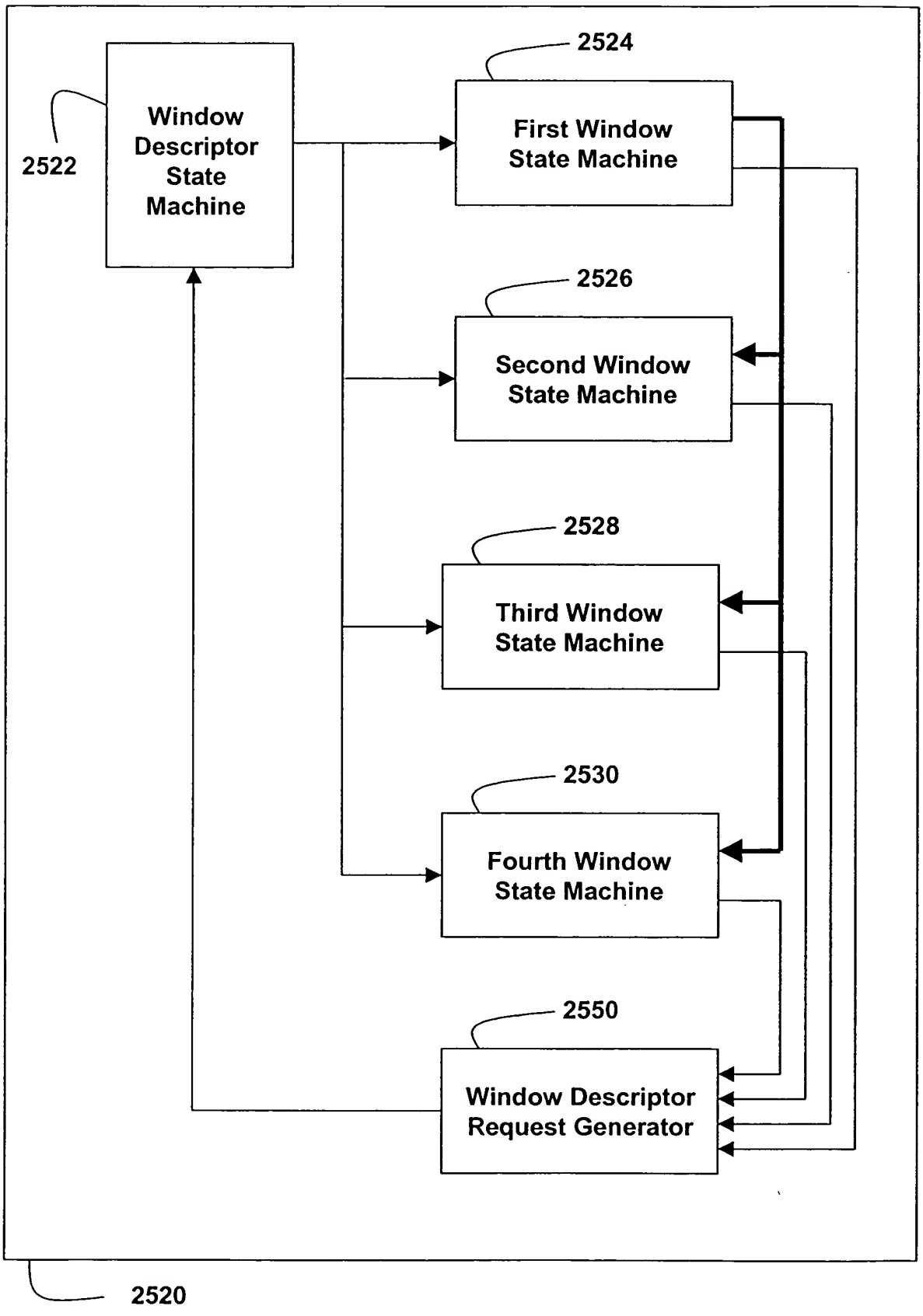
2524
Window Descriptor State Machine
2522
First Window State Machine
2526
Second Window State Machine
2528
Third Window State Machine
2530
Fourth Window State Machine
2550
Window Descriptor Request Generator
2520

FIG. 64

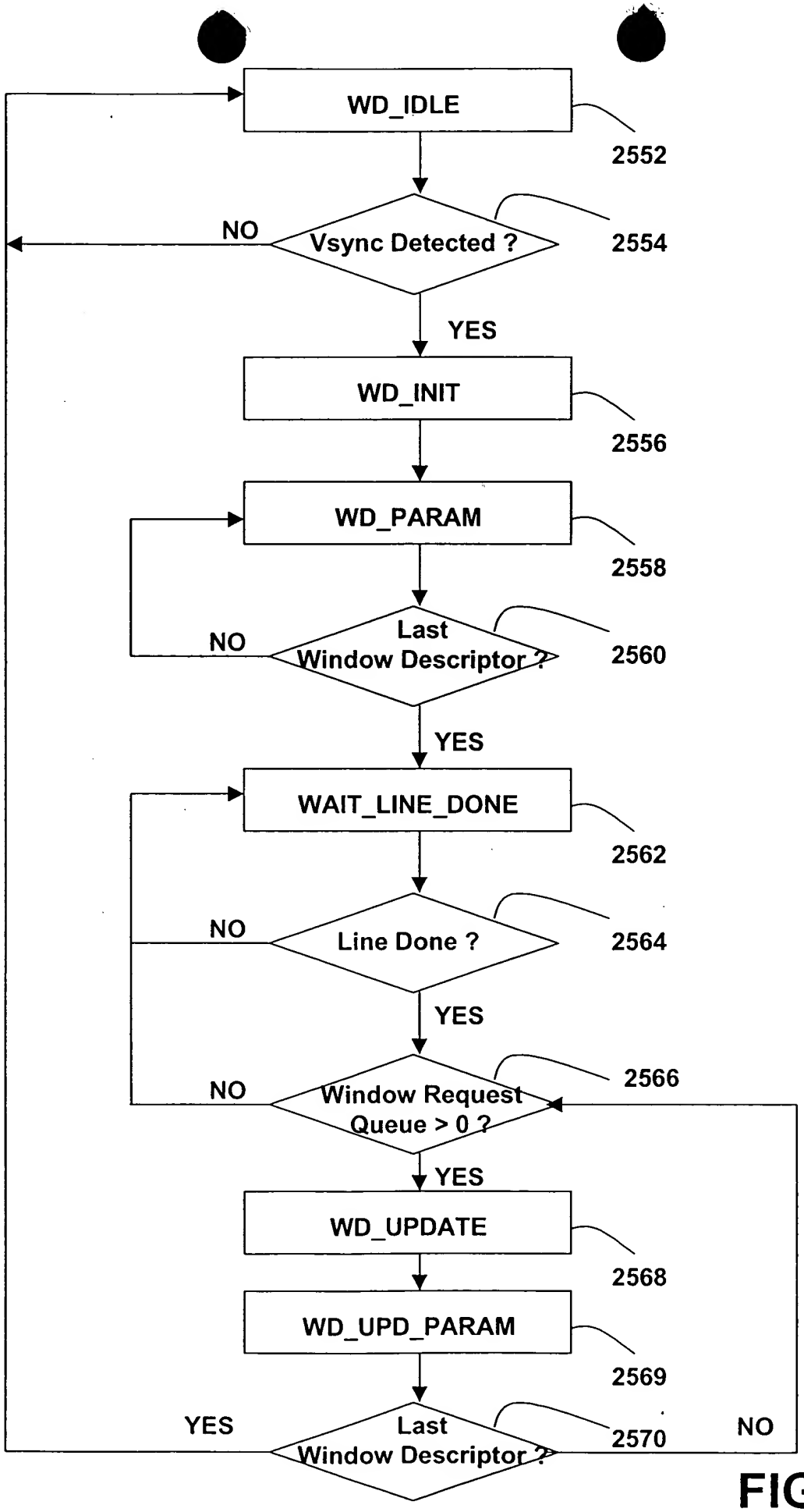
WD_IDLE
2552
NO
Vsync Detected ?
2554
YES
WD_INIT
2556
WD_PARAM
2558
NO
Last
Window Descriptor ?
2560
YES
WAIT_LINE_DONE
2562
NO
Line Done ?
2564
YES
2566
NO
Window Request
Queue > 0 ?
YES
WD_UPDATE
2568
WD_UPD_PARAM
2569
YES
Last
Window Descriptor ?
2570
NO

FIG. 65

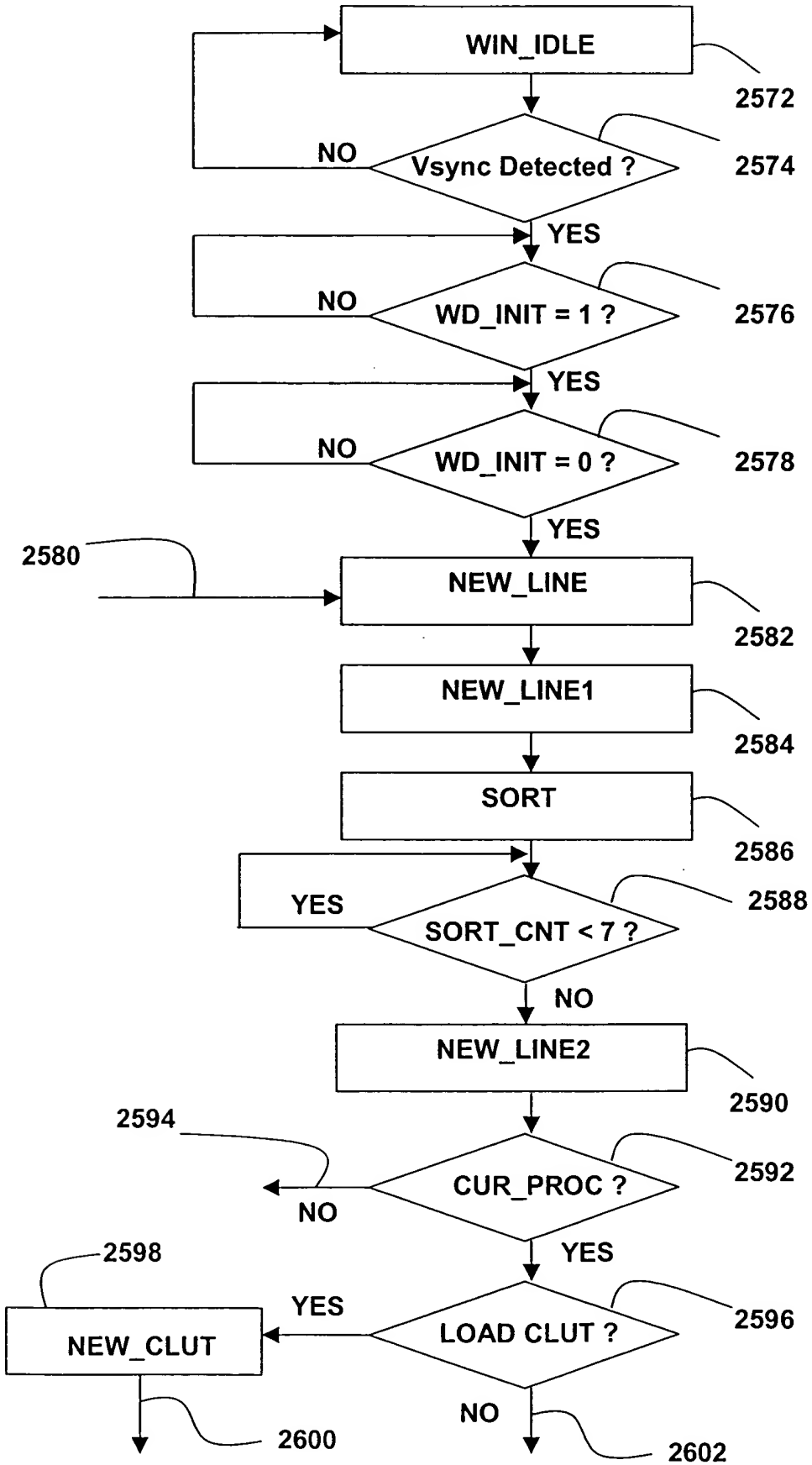
WIN_IDLE
2572
NO
Vsync Detected ?
2574
YES
NO
WD_INIT = 1 ?
2576
YES
NO
WD_INIT = 0 ?
2578
YES
2580
NEW_LINE
2582
NEW_LINE1
2584
SORT
2586
YES
SORT_CNT < 7 ?
2588
NO
NEW_LINE2
2590
2594
NO
CUR_PROC ?
2592
YES
2598
YES
NEW_CLUT
LOAD CLUT ?
2596
NO
2600
2602

FIG. 66

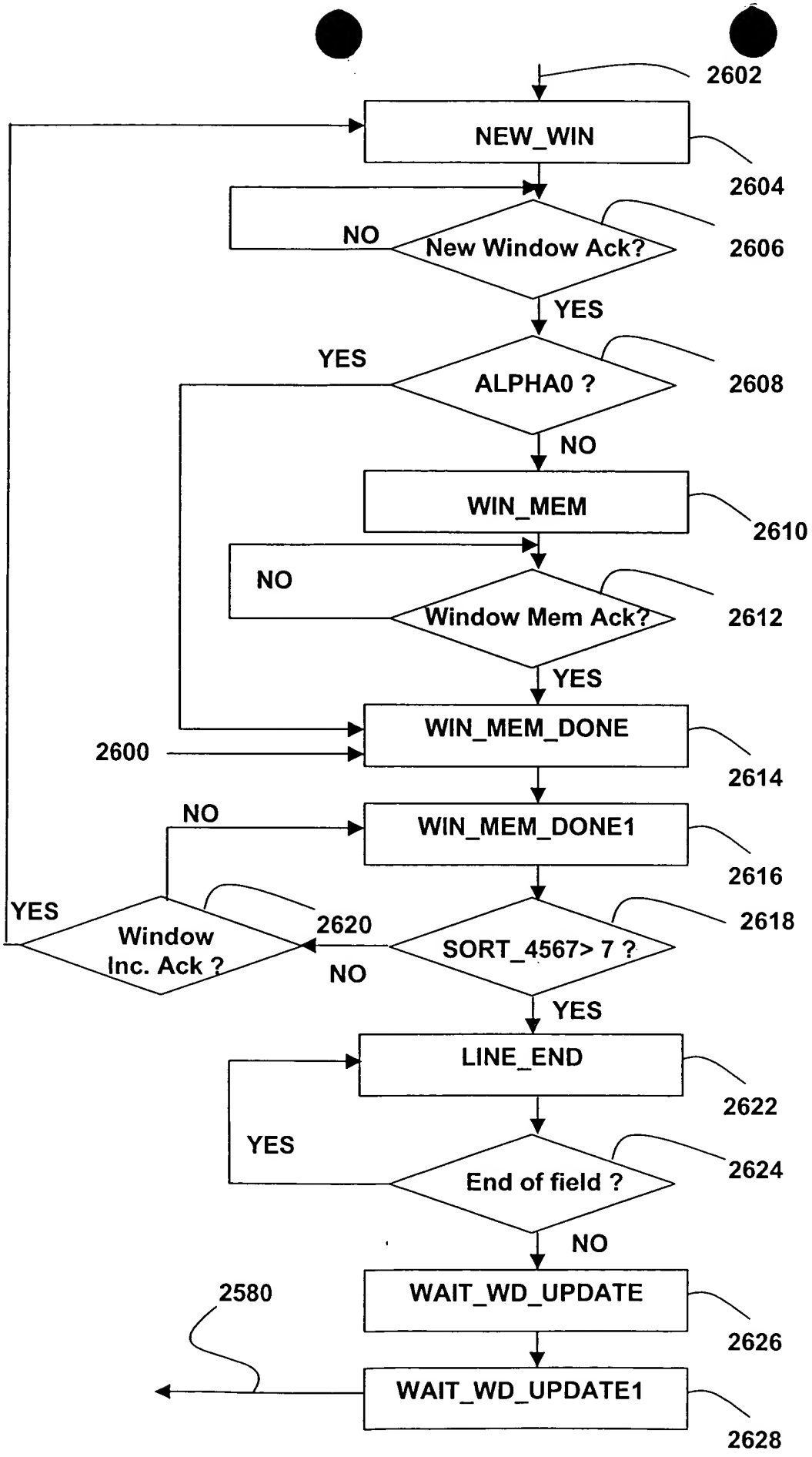
2602
NEW_WIN
2604
NO
New Window Ack?
2606
YES
YES
ALPHA0 ?
2608
NO
WIN_MEM
2610
NO
Window Mem Ack?
2612
YES
WIN_MEM_DONE
2600
2614
NO
WIN_MEM_DONE1
2616
YES
Window Inc. Ack ?
2620
SORT_4567> 7 ?
2618
NO
YES
LINE_END
2622
YES
End of field ?
2624
NO
2580
WAIT_WD_UPDATE
2626
WAIT_WD_UPDATE1
2628

FIG. 67

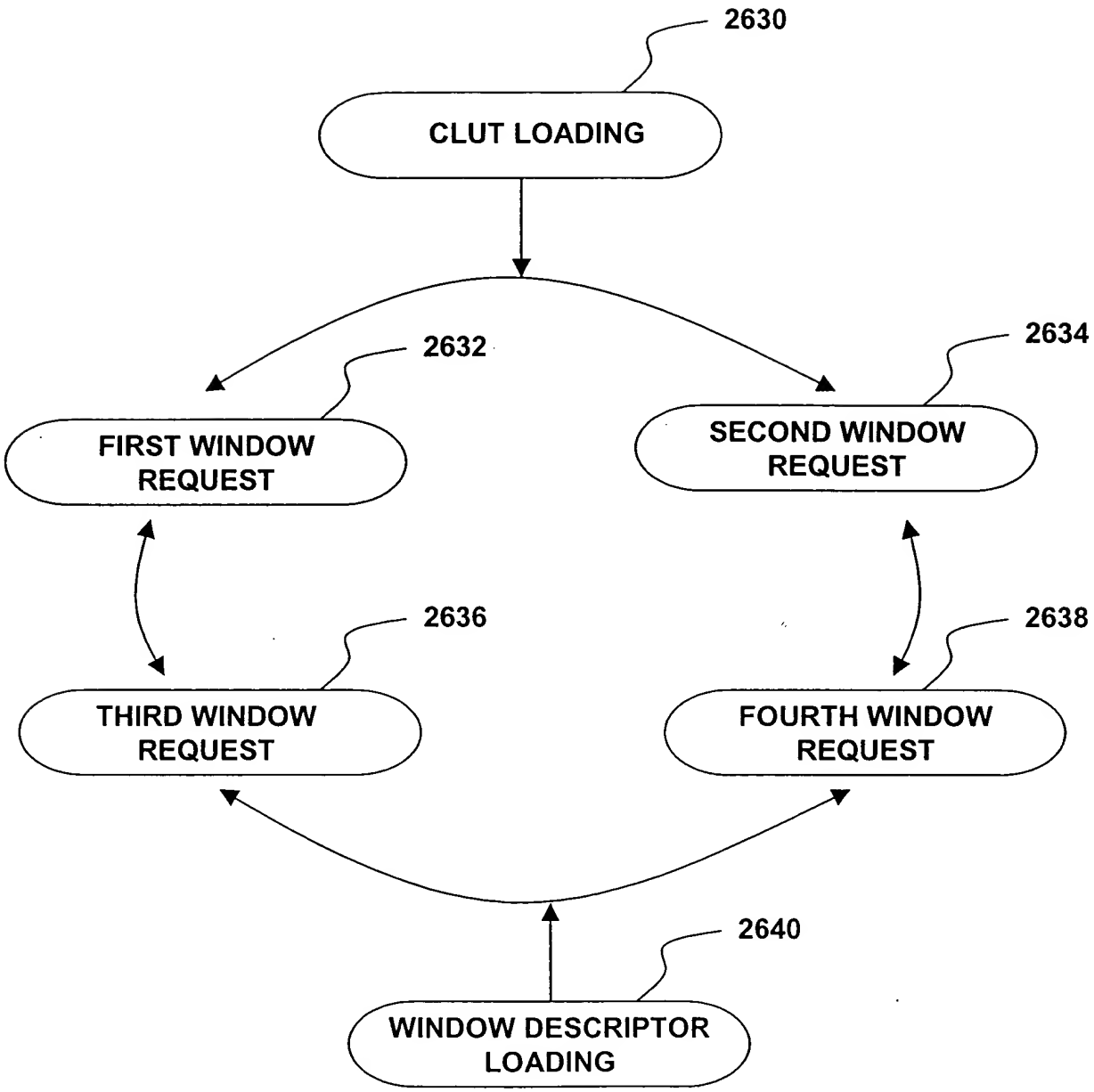
2630
CLUT LOADING
2632
FIRST WINDOW REQUEST
2634
SECOND WINDOW REQUEST
2636
THIRD WINDOW REQUEST
2638
FOURTH WINDOW REQUEST
2640
WINDOW DESCRIPTOR LOADING

FIG. 68

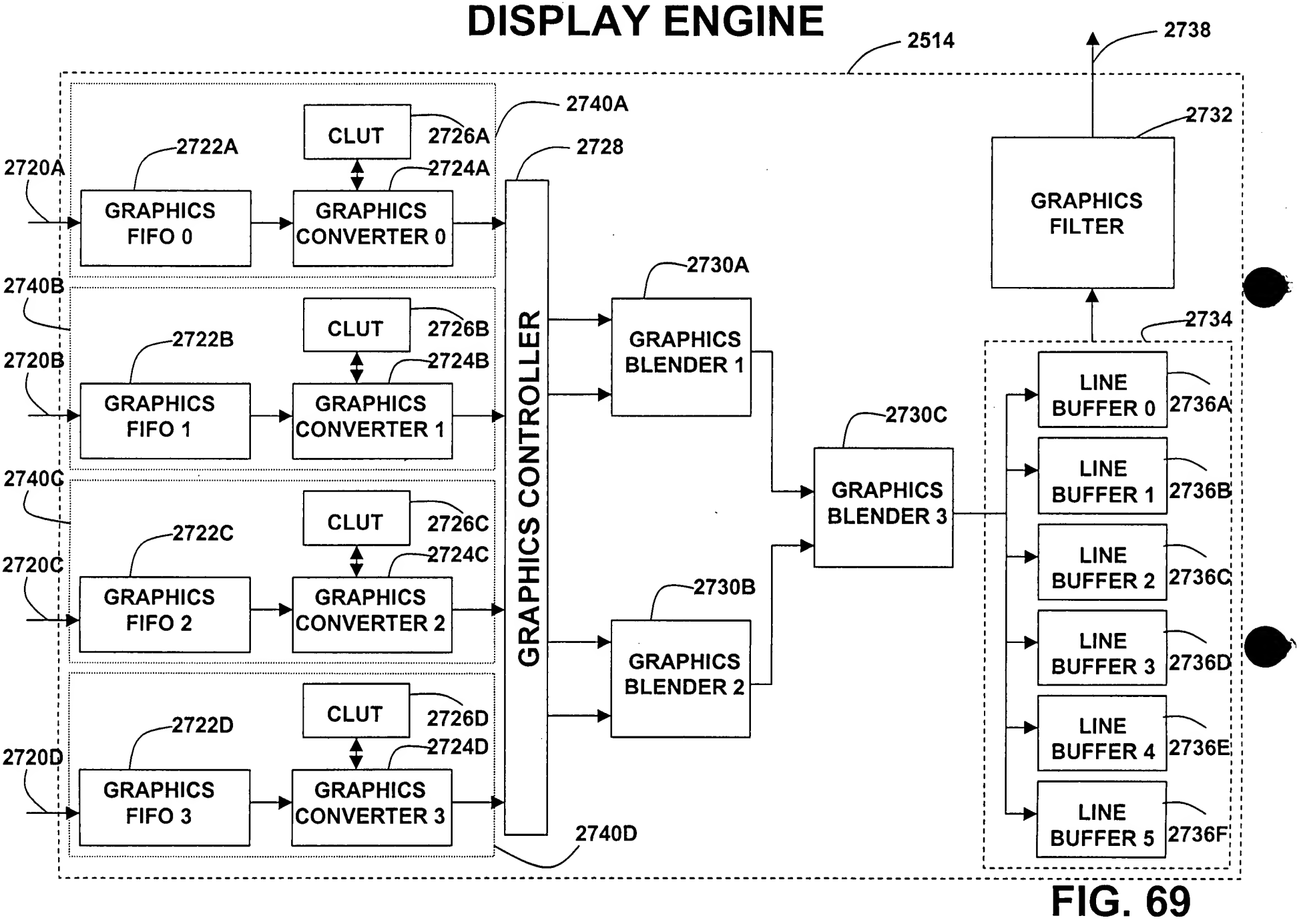

FIG. 69

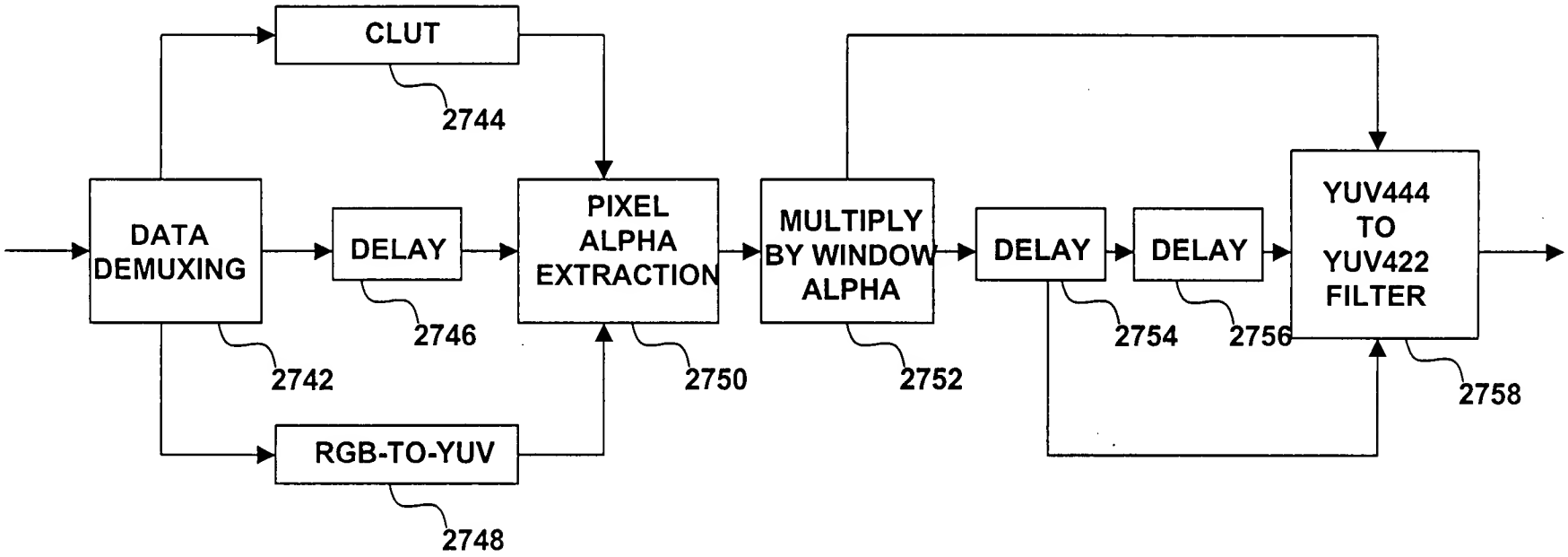

FIG. 70

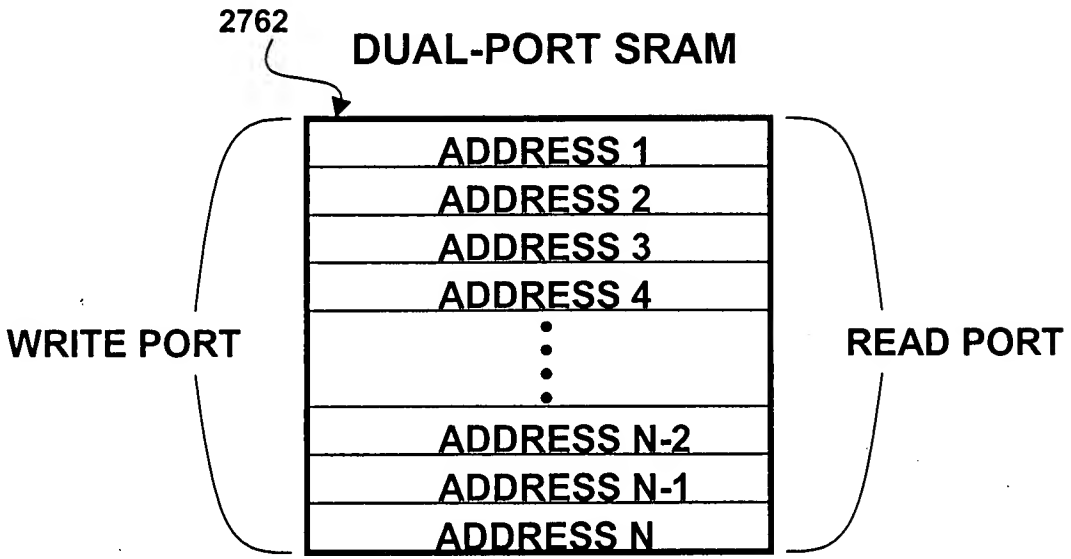

FIG. 71

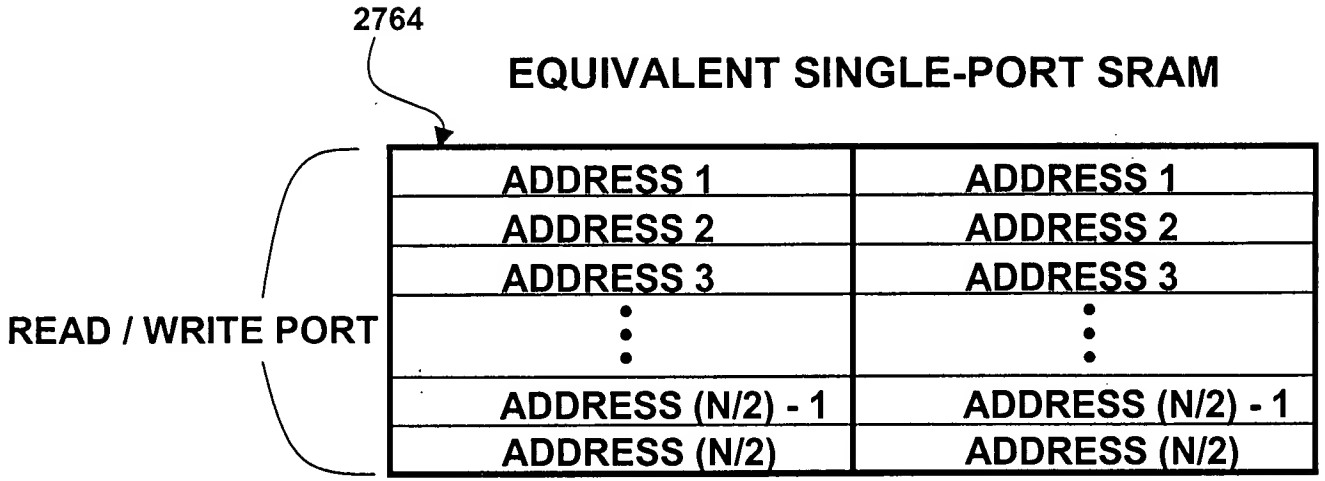

FIG. 72

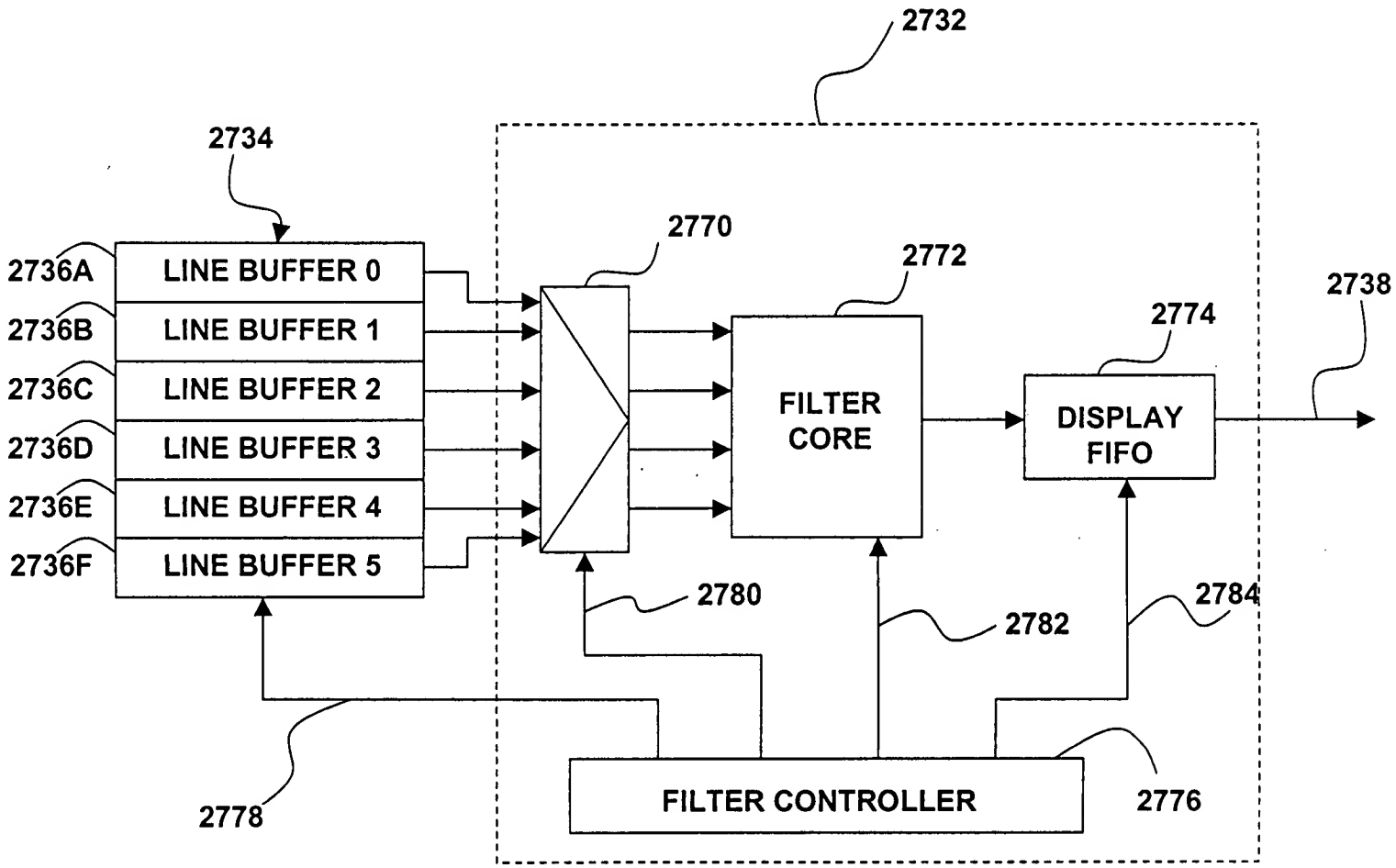

FIG. 73

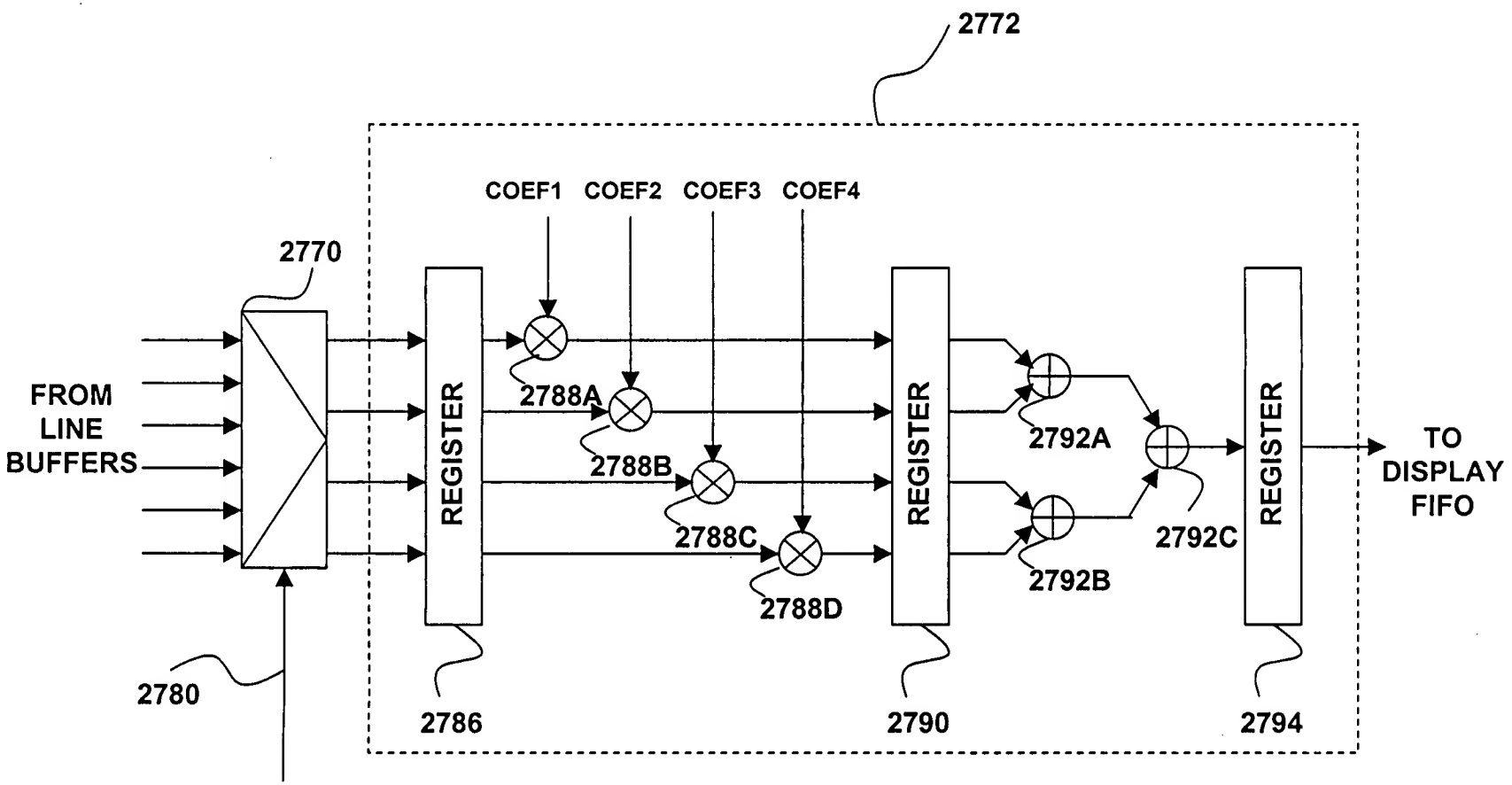

FIG. 74